

(12)

EUROPEAN PATENT APPLICATION

(43) Date of publication:
 05.01.2000 Bulletin 2000/01

(51) Int. Cl.⁷: G11C 11/24, G11C 27/02,
 G06K 9/00, G01R 27/26

(21) Application number: 99250215.3

(22) Date of filing: 01.07.1999

(84) Designated Contracting States:

AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU
 MC NL PT SE

Designated Extension States:

AL LT LV MK RO SI

(30) Priority: 04.06.1999 JP 15776399

04.06.1999 JP 15775599

20.08.1998 JP 23386798

20.08.1998 JP 23385898

08.07.1998 JP 19345598

02.07.1998 JP 18722798

19.08.1998 JP 23268998

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(54) Small capacitance change detection device

(57) A small capacitance change detection device includes a capacitance detection element, signal generation circuit, signal amplification circuit, and output circuit. The signal amplification circuit includes a first transistor and first to third voltage sources. The second or third voltage source is connected to the other output terminal of the first transistor via a first switch. A voltage to be applied from the second voltage source to the other output terminal is set to have a value equal to or larger than a value obtained by subtracting a threshold voltage of the first transistor from a voltage of the first voltage source while a voltage to be applied from the third voltage source to the other output terminal is set to have a value equal to or smaller than a value obtained by subtracting the threshold voltage from the voltage of the first voltage source. The output circuit is connected to a connection point between the other output terminal of the first transistor and the first switch and, after a voltage of the second or third voltage source is applied to the connection point in an ON state of the first switch, receives the voltage at the connection point on the basis of an OFF state of the first switch and charge control by the signal generation circuit after the first switch is turned off.

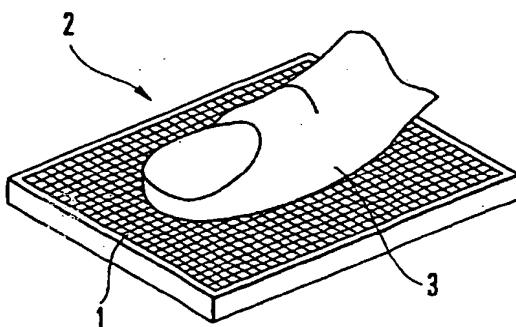


FIG. 1

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DescriptionBackground of the Invention

5 [0001] The present invention relates to a small capacitance change detection device and, more particularly, to a small capacitance change detection device for detecting a surface shape having a small three-dimensional pattern of, e.g., the skin surface of a human finger or nose of an animal as a small change in capacitance.

10 [0002] As sensors for recognizing a surface shape having a small three-dimensional pattern, especially, devices aiming at fingerprint detection have been reported. As a technique of detecting a fingerprint pattern, a capacitive detection type sensor using the LSI manufacturing technology has been proposed. This is described in, e.g., "ISSCC DIGEST OF TECHNICAL PAPERS", FEBRUARY 1998 pp. 284 - 285.

15 [0003] A capacitive detection type sensor senses the three-dimensional pattern of the skin surface of a finger by detecting an electrostatic capacitance generated between the electrodes of small sense units two-dimensionally arrayed on an LSI chip and the skin of a finger in contact with the electrodes via an insulating film. Since the capacitance value changes depending on the three-dimensional pattern on the skin surface of a finger, the three-dimensional pattern of the skin surface of a finger can be sensed by detecting the small capacitance difference.

20 [0004] Fig. 54 shows the basic arrangement of a conventional small capacitance change detection device using this principle. This small capacitance change detection device has a detection element 310 formed from an electrostatic capacitance between an electrode and skin of a finger in contact with the electrode via an insulating film, signal generation circuit 320 for generating a voltage signal corresponding to the electrostatic capacitance value of the detection element 310, and output circuit 340 for converting the voltage signal from the signal generation circuit 320 and outputting a signal.

25 [0005] Figs. 55A and 55B show the layout of the conventional small capacitance change detection device. This small capacitance change detection device has a plurality of detection elements 310, a plurality of signal generation circuits 320, and a plurality of output circuits 340. One detection element 310 and one signal generation circuit 320 construct a sense unit 301. The sense units 301 are two-dimensionally arrayed on an LSI chip to form a sensor array 302. The output circuits 340 are arranged near the sensor array 302 to form an output section 304.

30 [0006] Since the electrostatic capacitance value of each detection element 310 is determined depending on the distance between the electrode of the sense unit 301 and skin surface of a finger, the electrostatic capacitance value of the detection element 310 changes depending on the three-dimensional pattern of the skin surface of the finger. When a finger is depressed against the sensor array 302, each sense unit 301 outputs a voltage signal corresponding to the three-dimensional pattern of the skin surface of the finger. This voltage signal is converted into a desired signal reflecting the three-dimensional pattern of the skin surface of the finger, so the fingerprint pattern is detected.

35 [0007] The arrangement and operation of the conventional small capacitance change detection device shown in Fig. 54 will be described below in more detail.

40 [0008] Fig. 56 shows the circuit arrangement of the conventional small capacitance change detection device. Referring to Fig. 56, reference symbol C_f denotes an electrostatic capacitance formed between the electrode of the sense unit 301 and the skin surface of a finger in contact with the electrode via an insulating film. The electrode of the sense unit 301 is connected to the input side of a current source 321 of a current I through an NMOS transistor Q3. A node N1 between the electrode and transistor Q3 is connected to the input side of the output circuit 340. A power supply voltage VDD is applied to the node N1 through a PMOS transistor Q1. The node N1 has a parasitic capacitance $Cp1$. Signals \overline{PRE} and RE are supplied to the gate terminals of the transistors Q1 and Q3, respectively.

45 [0009] The capacitance C_f forms the detection element 310. The current source 321 and transistor Q3 construct the signal generation circuit 320.

[0010] Figs. 57A to 57C explain the operation of the small capacitance change detection device shown in Fig. 56.

[0011] First, the signal \overline{PRE} of high level (VDD) is supplied to the gate terminal of the transistor Q1, and the signal RE of low level (GND) is supplied to the gate terminal of the transistor Q3. Hence, both the transistors Q1 and Q3 are OFF.

50 [0012] In this state, when the signal \overline{PRE} changes from high level to low level, the transistor Q1 is turned on. Since the transistor Q3 is kept off, the node N1 is precharged to VDD.

[0013] After precharge, the signal \overline{PRE} goes high, and simultaneously, the signal RE goes high. The transistor Q1 is turned off, and the transistor Q3 is turned on. Charges stored at the node N1 are removed from the current source 321. As a result, the potential at the node N1 lowers.

55 [0014] Letting Δt be the period while the signal RE is at high level, a potential drop ΔV at the node N1 after the period Δt elapses is given by $I \Delta t / (C_f + Cp1)$.

[0015] Since the current I , period Δt , and parasitic capacitance $Cp1$ are constant, the potential drop ΔV is determined by the capacitance C_f . Since the capacitance C_f is determined by the distance between the electrode of the sensor and the skin surface of a finger, the value of the capacitance C_f changes depending on the three-dimensional pattern of the

skin surface of a finger. This means that the magnitude of the potential drop ΔV changes reflecting the three-dimensional pattern of the skin surface of a finger. This potential drop ΔV is supplied to the output circuit 340 as an input signal. The output circuit 340 identifies the magnitude of the potential drop ΔV and outputs a signal reflecting the three-dimensional pattern of the skin surface of a finger.

5 [0016] In the conventional small capacitance change detection device, however, when the parasitic capacitance $Cp1$ at the node N1 is large, the potential drop ΔV becomes small. When the circuit shown in Fig. 56 is arranged using the LSI manufacturing technology in practice, the parasitic capacitance $Cp1$ becomes larger than the capacitance Cf .

10 [0017] The potential drop ΔV can be made large by increasing the current I of the current source 321 or period Δt of the signal RE at high level. However, when the current I is large, the sense units 301 with manufacturing variations are hard to control. For this reason, the current I is preferably relatively small to obtain high detection accuracy. Also, the period Δt cannot be made so long from the viewpoint of the detection time.

15 [0018] Consequently, the potential drop ΔV as a signal to be input to the output circuit 340 becomes small, and the output varies due to noise margin or manufacturing variations, resulting in a decrease in surface shape detection accuracy.

20 [0019] Hence, as described above, a signal change reflecting the three-dimensional pattern of a skin surface of a finger decreases due to the influence of a parasitic element such as the parasitic capacitance $Cp1$ formed in the manufacturing process, and the detection accuracy of the small capacitance change detection device becomes low.

Summary of the Invention

20 [0020] It is therefore an object of the present invention to accurately extract a small change in capacitance by a small capacitance change detection device.

25 [0021] It is another object of the present invention to increase the design margin of the output circuit of a small capacitance change detection device.

30 [0022] In order to achieve the above objects, according to the present invention, there is provided a small capacitance change detection device comprising a capacitance detection element for detecting a small capacitance change, a signal generation circuit having an output side connected to the capacitance detection element to control predetermined charges, a signal amplification circuit having an input side connected to a connection point between the output side of the signal generation circuit and the capacitance detection element, and an output circuit connected to an output side of the signal amplification circuit, the signal amplification circuit comprising a first transistor having one output terminal connected to the connection portion between the output side of the signal generation circuit and the capacitance detection element, a first voltage source connected to a control terminal of the first transistor, a second voltage source, and a third voltage source, wherein one of the second and third voltage sources is connected to the other output terminal of the first transistor via a first switch, a voltage to be applied from the second voltage source to the other output terminal of the first transistor is set to have a value not less than a value obtained by subtracting a threshold voltage of the first transistor from a voltage of the first voltage source that is applied to the control terminal of the first transistor while a voltage to be applied from the third voltage source to the other output terminal of the first transistor is set to have a value not more than a value obtained by subtracting the threshold voltage of the first transistor from the voltage of the first voltage source that is applied to the control terminal of the first transistor, and the output circuit is connected to a connection point between the other output terminal of the first transistor and the first switch and, after a voltage of one of the second and third voltage sources is applied to the connection point in an ON state of the first switch, receives the voltage at the connection point on the basis of an OFF state of the first switch and charge control by the signal generation circuit after the first switch is turned off.

45 Brief Description of the Drawings

[0023]

50 Fig. 1 is a perspective view showing a small capacitance change detection device according to the first embodiment of the present invention;

Fig. 2 is a block diagram showing the arrangement of a sense unit of the device shown in Fig. 1;

Fig. 3 is a sectional view showing the arrangement of the detection element of the device shown in Fig. 1;

Fig. 4 is a circuit diagram of the sense unit shown in Fig. 2;

55 Figs. 5A to 5C are timing charts showing the operation of the sense unit shown in Fig. 4;

Fig. 6 is a circuit diagram showing another arrangement of the sense unit shown in Fig. 2;

Figs. 7 is a block diagram of a sense unit according to the second embodiment of the present invention;

Fig. 8 is a circuit diagram of the sense unit shown in Fig. 7;

Figs. 9A to 9C are timing charts showing the operation of the sense unit shown in Fig. 8;

Fig. 10 is a circuit diagram of a sense unit according to the third embodiment of the present invention;
 Fig. 11 is a circuit diagram of a sense unit according to the fourth embodiment of the present invention;
 Fig. 12 is a circuit diagram of a sense unit according to the fifth embodiment of the present invention;
 Fig. 13 is a circuit diagram of a sense unit according to the sixth embodiment of the present invention;
 5 Figs. 14A to 14C are timing charts showing the operation of the sense unit shown in Fig. 13;
 Figs. 15A to 15C are block diagrams showing the seventh embodiment of the present invention;
 Fig. 16 is a block diagram showing the eighth embodiment of the present invention;
 10 Figs. 17A and 17B are circuit diagrams of signal amplification circuits according to the ninth embodiment of the present invention;
 Figs. 18A and 18B are a sectional view and equivalent circuit diagram, respectively, showing a surface shape recognition sensor according to the 10th embodiment of the present invention;
 Fig. 19 is a plan view of the surface shape recognition sensor;
 Fig. 20 is a sectional view showing deformation of the surface shape recognition sensor;
 15 Fig. 21 is a graph showing a capacitance Cf and capacitance Cr of the surface shape recognition sensor;
 Fig. 22 is a block diagram showing the 11th embodiment of the present invention;
 Figs. 23A to 23C are timing charts showing the operation of the device shown in Fig. 22;
 Fig. 24 is a graph showing the characteristics of the device shown in Fig. 22;
 Fig. 25 is a graph showing the characteristics of the device shown in Fig. 22;
 20 Fig. 26 is a graph showing the characteristics of the device shown in Fig. 22;
 Fig. 27 is a block diagram showing the 12th embodiment of the present invention;
 Fig. 28 is a circuit diagram of the device shown in Fig. 27;
 Figs. 29A to 29D are timing charts showing the operation of the device shown in Fig. 27;
 Fig. 30 is a block diagram showing the 13th embodiment of the present invention;
 Fig. 31 is a circuit diagram of the device shown in Fig. 30;
 25 Fig. 32 is a circuit diagram of a variable threshold circuit arranged in the output circuit of the device shown in Fig. 31;
 Fig. 33 is a block diagram showing the 14th embodiment of the present invention;
 Fig. 34 is a circuit diagram of the device shown in Fig. 33;
 Fig. 35 is a block diagram showing the 15th embodiment of the present invention;
 30 Fig. 36 is a block diagram showing the 16th embodiment of the present invention;
 Fig. 37 is a block diagram showing the 17th embodiment of the present invention;
 Fig. 38 is a circuit diagram of a variable threshold circuit according to the 18th embodiment of the present invention;
 Fig. 39 is a block diagram showing a connection example of the variable threshold circuit shown in Fig. 38;
 35 Fig. 40 is a graph showing operation waveforms by the circuit arrangement shown in Fig. 39;
 Fig. 41 is a circuit diagram of a variable threshold circuit according to the 19th embodiment of the present invention;
 Fig. 42 is a block diagram showing a connection example of the variable threshold circuit shown in Fig. 41;
 Fig. 43 is a circuit diagram of a variable threshold circuit according to the 20th embodiment of the present invention;
 40 Fig. 44 is a circuit diagram of a variable threshold circuit according to the 21st embodiment of the present invention;
 Fig. 45 is a circuit diagram of a variable threshold circuit according to the 24th embodiment of the present invention;
 Fig. 46 is a view showing the 27th embodiment of the present invention;
 Figs. 47A to 47C are timing charts showing the operation of the device shown in Fig. 46;
 45 Fig. 48 is a graph showing comparison of a signal change reflecting the three-dimensional pattern of the surface shape of a measurement object between the device in Fig. 46 and conventional device;
 Fig. 49 is a view showing the 28th embodiment of the present invention;
 Figs. 50A to 50C are timing charts showing the operation of the device shown in Fig. 49;
 Fig. 51 is a graph showing comparison of a signal change reflecting the three-dimensional pattern of the surface shape of a measurement object between the device in Fig. 49 and conventional device;
 50 Fig. 52 is a block diagram of a sense unit according to the 29th embodiment of the present invention;
 Figs. 53A to 53C are block diagrams showing other arrangements of the sense unit shown in Fig. 52;
 Fig. 54 is a block diagram showing a conventional device;
 Figs. 55A and 55B are views showing the layout of the device shown in Fig. 54;
 Fig. 56 is a circuit diagram of the device shown in Fig. 54; and
 Figs. 57A to 57C are timing charts showing the operation of the device shown in Fig. 56.

55 Description of the Preferred Embodiments

[0024] Embodiments of the present invention will be described below in detail with reference to the accompanying drawings.

(First Embodiment)

[0025] Fig. 1 shows a small capacitance change detection device according to the first embodiment of the present invention. This device has sense units 1 as constituent units, as shown in Fig. 1. The sense units 1 are arrayed in a matrix on an LSI chip to form a sensor array 2.

[0026] Fig. 2 shows the arrangement of each sense unit 1 shown in Fig. 1. The sense unit 1 comprises a detection element 10 whose quantity of electricity changes in accordance with contact of a recognition object such as a human finger 3, first signal generation circuit 20 for generating a signal corresponding to the quantity of electricity of the detection element 10, signal amplification circuit 30 for amplifying the level of the signal from the signal generation circuit 20 and outputting the signal, and output circuit 40 for converting the output signal from the signal amplification circuit 30 into a desired signal and outputting the signal, as shown in Fig. 2.

[0027] Fig. 2 shows the small capacitance change detection device using the detection element 10 comprising an electrostatic capacitance formed between the sensor electrode of the sense unit 1 and skin surface of the finger 3. In this case, the node between the detection element 10 and signal generation circuit 20 is connected to the input side of the signal amplification circuit 30, and the output circuit 40 is connected to the output side of the signal amplification circuit 30.

[0028] Fig. 3 shows the arrangement of the detection element 10 shown in Fig. 2. An insulating underlayer 12 is formed on a semiconductor substrate 11 having an LSI or the like. Interconnections 13 are formed on the insulating underlayer 12. An interlevel insulating layer 14 is formed on the interconnections 13 and insulating underlayer 12. Sensor electrodes 16 each having, e.g., a rectangular shape are formed on the interlevel insulating layer 14. The sensor electrodes 16 are connected to the interconnections 13 via plugs 15 in through holes formed in the interlevel insulating layer 14. A passivation film 17 is formed on the interlevel insulating layer 14 to cover the sensor electrodes 16.

[0029] Although not illustrated, the signal generation circuit 20 and signal amplification circuit 30 shown in Fig. 2 are connected to the interconnections 13.

[0030] In this arrangement, when the finger 3 for a target fingerprint is depressed against the sensor array 2 and comes into contact with the passivation film 17, the skin surface of the finger 3 in contact with the passivation film 17 on the sensor electrodes 16 functions as an electrode, so an electrostatic capacitance is formed between the skin surface and sensor electrodes 16.

[0031] The skin surface at a finger tip is formed by ridge and valley portions. For this reason, when the finger 3 is brought into contact with the passivation film 17, the distance between the skin surface as an electrode and sensor electrode 16 changes between the valley and ridge portions of the skin surface. This difference in distance is detected as a capacitance difference.

[0032] In each sense unit 1, a signal corresponding to the capacitance of the detection element 10 is output from the signal generation circuit 20. This signal is amplified in its level by the signal amplification circuit 30, converted into a desired signal by the output circuit 40, and output from the sense unit 1.

[0033] The signals output from the sense units 1 reflect the ridge and valley portions of the skin surface. Hence, the fingerprint pattern can be detected on the basis of these signals.

[0034] The small capacitance change detection device shown in Fig. 1 may be formed on an LSI chip which integrates a storage section storing fingerprint data for collation and a recognition processing section for comparing and collating 40 fingerprint data prepared in the storage section with a fingerprint pattern detected by a surface shape recognition sensor circuit.

[0035] When these components are formed on one LSI chip, information is hardly be altered in data transmission, and confidentiality can be improved.

[0036] The sense unit 1 shown in Fig. 2 will be described next in more detail.

[0037] Fig. 4 shows the sense unit 1. Referring to Fig. 4, reference symbol C_f denotes an electrostatic capacitance formed between the sensor electrode 16 in Fig. 3 and the skin surface of the finger 3. The sensor electrode 16 forming the capacitance C_f is connected to the drain terminal of an NMOS transistor Q3a. The source terminal of the transistor Q3a is connected to the input side of a current source 21a of a current I . The source terminal of an NMOS transistor Q2a is connected to a node N1a between the sensor electrode 16 and transistor Q3a. The drain terminal of the transistor Q2a is connected to the drain terminal of a PMOS transistor Q1a having a source terminal applied with a power supply voltage VDD and the gate terminal of an NMOS transistor Q4a having a drain terminal applied with the power supply voltage VDD and source terminal connected to ground through a resistance Ra. The source terminal of the transistor Q4a is connected to an inverter gate 41.

[0038] Signals PRE and RE are supplied to the gate terminals of the transistors Q1a and Q3a, respectively. A bias voltage VG is applied from a constant voltage source to the gate terminal of the transistor Q2a. Letting V_{th} be the gate-source threshold voltage for turning off the transistor Q2a, the voltages VDD and VG are set such that $VDD \geq VG - V_{th}$ is satisfied.

[0039] The nodes N1a and N2a have parasitic capacitances C_{p1a} and C_{p2a} , respectively.

[0040] The capacitance C_f constructs the detection element 10. The current source 21a and transistor Q3a construct the signal generation circuit 20. The transistors Q1a and Q2a construct the signal amplification circuit 30. The transistor Q4a, resistance R_a , and inverter gate 41 construct the output circuit 40. The small capacitance change detection device shown in Fig. 4 is different from the conventional device in that the transistor Q2a is inserted between the nodes N1a and N2a.

[0041] Figs. 5A to 5C explain operation of the sense unit 1 shown in Fig. 4. Fig. 5A shows the potential change in the signal PRE for controlling the transistor Q1a. Fig. 5B shows the potential change in the signal RE for controlling the transistor Q3a. Fig. 5C shows potential changes at the nodes N1a and N2a.

[0042] Referring to Fig. 4, the potentials at the nodes N1a and N2a are reset by a reset circuit (not shown) in advance and set at low level (GND) in the initial state, as shown in Fig. 5C. This reset circuit can be realized by, e.g., an NMOS transistor.

[0043] In this state, first, the signal PRE of high level (VDD) is supplied to the gate terminal of the transistor Q1a, and the signal RE of low level (GND) is supplied to the gate terminal of the transistor Q3a. Hence, both the transistors Q1a and Q3a are OFF.

[0044] In this state, when the signal PRE changes from high level to low level, the transistor Q1a is turned on. Since the transistor Q3a is kept off, and the signal generation circuit 20 is stopped, the node N2a is precharged to VDD.

[0045] The node N1a is charged until the gate-source voltage of the transistor Q2a reaches the threshold voltage V_{th} to turn off the transistor Q2a. Hence, the node N1a is precharged to $VG - V_{th}$.

[0046] After precharge, when the signal PRE goes high, the transistor Q1a is turned off. Simultaneously, the signal RE goes high to turn on the transistor Q3a, so the signal generation circuit 20 changes to an operative state. Charges stored at the node N1a are removed from the current source 21a to slightly lower the potential at the node N1a. The gate-source voltage of the transistor Q2a becomes higher than the threshold voltage V_{th} to turn on the transistor Q2a. With this operation, charges at the node N2a are also removed to start lowering the potential at the node N2a.

[0047] The parasitic capacitance C_{p2a} is mainly formed from the parasitic capacitances of the drain terminals of the transistors Q1a and Q2a and the parasitic capacitance of the gate terminal of the transistor Q4a. The parasitic capacitance C_{p2a} can be made considerably smaller than the parasitic capacitance C_{p1} of the conventional device by the actual layout.

[0048] For this reason, when potential drop at the node N2a begins, as described above, the potential at the node N2a abruptly lowers. After the potential at the node N2a equals that at the node N1a, the potential drop at the node N2a becomes moderate.

[0049] Letting Δt be the period while the signal RE is at high level, a potential drop ΔV at the node N1a after the period Δt is given by

$$\Delta V = VDD - (VG - V_{th}) + I\Delta t/(C_f + C_{p1a}) \quad (1)$$

The parasitic capacitance C_{p2a} is sufficiently smaller than the parasitic capacitance C_{p1a} .

[0050] In the small capacitance change detection device shown in Fig. 4, the magnitude of the potential drop ΔV can be made larger than that in the conventional device by $VDD - (VG - V_{th})$. For this reason, even when the parasitic capacitance C_{p1a} at the node N1a is large, the potential drop ΔV becomes large.

[0051] In the output circuit 40, the current flowing between the source and drain of the transistor Q4a changes depending on the potential drop ΔV as an input signal. This current change is converted into a voltage change by the resistance R_a .

[0052] The inverter gate 41 converts a signal into a digital signal using a predetermined logic threshold value. More specifically, when the input voltage value to the inverter gate 41 is smaller than the threshold value, the inverter gate 41 outputs a signal representing that a valley portion is in contact with the sense unit 1. Conversely, when the input voltage value to the inverter gate 41 is larger than the threshold value, the inverter gate 41 outputs a signal representing that a ridge portion is in contact with the sense unit 1.

[0053] When the potential drop ΔV at the node N2a becomes larger by $VDD - (VG - V_{th})$, the threshold value setting width of the inverter gate 41 increases. Since the threshold value can be set to prevent the inverter gate 41 from erroneously operating due to noise, the detection accuracy of the device can be improved.

[0054] The sense unit 1 shown in Fig. 4 is constituted by the detection element 10, signal generation circuit 20, signal amplification circuit 30, and output circuit 40. Since the signal generation circuit 20 and signal amplification circuit 30 are arranged near the corresponding detection element 10, the parasitic element such that the parasitic capacitance C_{p1a} connected to the detection element 10 becomes small.

[0055] Additionally, since the output circuit 40 is arranged near the corresponding signal amplification circuit 30, the parasitic capacitance C_{p2a} between the signal amplification circuit 30 and output circuit 40 becomes small.

[0056] Since the parasitic elements that are formed in the manufacturing process and contribute to signal attenuation can be suppressed, the input signal (ΔV) to the output circuit 40 can be made larger.

[0057] Another element may be used in place of the inverter gate 41, as needed. For example, when an analog signal corresponding to the quantity of electricity of the detection element 10 is to be output from the output circuit 40, an analog amplification circuit is applied. To convert a signal corresponding to the quantity of electricity of the detection element 10 into a digital value, an A/D converter is used. When data is sampled using, e.g., a latch circuit controlled by a clock signal, the signal amount can be made to correspond to the time axis.

[0058] The detection element 10 may be the capacitance Cf which has a pair of sensor electrodes opposing each other via an insulating film and whose value changes when the upper electrode displaces in the vertical direction in accordance with the ridges and valley portions of the skin surface of a finger.

[0059] In place of the signal generation circuit 20 using the current source 21a, a first signal generation circuit 22 constructed by using a capacitance Cs as shown in Fig. 6 may be used. In this signal generation circuit 22, one fixed terminal of a switch SW1 is connected to the detection element 10, the other fixed terminal is connected to ground, and the movable terminal is connected to the capacitance Cs.

[0060] In the signal generation circuit 22, the switch SW1 connects the capacitance Cs to ground in the ON state of the transistor Q1a in Fig. 4 to remove charges from the capacitance Cs in advance. In the OFF state of the transistor Q1a, the switch SW1 connects the capacitance Cs to the detection element 10 to store a predetermined amount of charges in the capacitance Cs, thereby generating a signal corresponding to the amount of electricity of the detection element 10.

(Second Embodiment)

[0061] Fig. 7 shows a sense unit 1 constructing a small capacitance change detection device according to the second embodiment of the present invention. The same reference numerals as in Fig. 2 denote the same parts in Fig. 7, and a detailed description thereof will be omitted.

[0062] The sense unit 1 shown in Fig. 7 is different from the sense unit 1 shown in Fig. 2 in that the sense unit 1 has a reference signal generation circuit 50 for generating a reference signal, and a signal amplification circuit 31 has a means for changing the gain on the basis of the level of the signal from a signal generation circuit 20 and that of the reference signal.

[0063] Fig. 8 shows the sense unit 1 shown in Fig. 7. The same reference numerals as in Fig. 4 denote the same parts in Fig. 8, and a detailed description thereof will be omitted.

[0064] The sense unit 1 shown in Fig. 8 is formed by adding a reference element 51, second signal generation circuit 52, NMOS transistor Q2b, and PMOS transistor Q1b to the sense unit 1 shown in Fig. 4.

[0065] The reference element 51 is a simulated detection element 10. In the sense unit 1 shown in Fig. 8, since the detection element 10 is formed by a capacitance Cf, the reference element 51 is formed by a capacitance Cr.

[0066] The capacitance Cr is used as a threshold value for determining whether a ridge or valley portion of the skin surface of a finger is in contact with the sense unit 1. The value of the capacitance Cr is set between the capacitance Cf formed when a ridge portion of the skin surface of a finger is in contact with the sense unit 1 and that formed when a valley portion of the skin surface of a finger is in contact with the sense unit 1. The capacitance Cr effectively functions as a threshold value even when it is set to equal the value of the capacitance Cf formed when a valley portion of the skin surface of a finger is in contact.

[0067] The capacitance Cr is formed by an element or semiconductor element formed using interconnections. For example, the capacitance Cr can be realized by a MIM (metal-Insulator-Metal) capacitance or PIP (Polysilicon-Insulator-Polysilicon) capacitance formed by inserting an insulating film between interconnections, or a MOS capacitance.

[0068] The signal generation circuit 52 generates a reference signal corresponding to the capacitance Cr and has the same circuit arrangement as that of the signal generation circuit 20. More specifically, the signal generation circuit 52 comprises a current source 21b and NMOS transistor Q3b, which have the same characteristics as those of a current source 21a and transistor Q3a of the signal generation circuit 20, respectively.

[0069] The reference signal generation circuit 50 is constructed by the reference element 51 and signal generation circuit 52. The reference signal generated by the reference signal generation circuit 50 has the same level as that of a signal generated by the signal generation circuit 20 when the detection element 10 has a capacitance set as a threshold value.

[0070] A node N1b between the reference element 51 and signal generation circuit 52 is connected to the source terminal of the NMOS transistor Q2b. The drain terminal of the transistor Q2b is connected to the drain terminal of the PMOS transistor Q1b with a source terminal applied with a power supply voltage VDD.

[0071] In the sense unit 1 shown in Fig. 4, the gate terminal of the transistor Q2a is connected to the constant voltage source. In the sense unit 1 shown in Fig. 8, however, the gate terminal of a transistor Q2a is connected to the drain terminal of the transistor Q2b. The gate terminal of the transistor Q2b is connected to the drain terminal of the transistor Q2a.

[0072] The PMOS transistors Q1b and Q2b have the same characteristics as those of the transistors Q1a and Q2a,

respectively.

[0073] Signals PRE and RE are supplied to the gate terminals of the PMOS transistors Q1b and Q3b, respectively.

[0074] The nodes N1b and N2b have parasitic capacitances Cp1b and Cp2b, respectively.

[0075] The transistors Q1a and Q1b construct a second switch means. The second switch means and transistors Q2a and Q2b construct the signal amplification circuit 31.

5 [0076] Figs. 9A to 9C explain operation of the sense unit 1 shown in Fig. 8. Fig. 9A shows the potential change in the signal PRE for controlling the transistors Q1a and Q1b. Fig. 9B shows the potential change in the signal RE for controlling the transistors Q3a and Q3b. Fig. 9C shows potential changes at the node N2a.

10 [0077] Referring to Fig. 8, the potentials at the nodes N1a, N2a, N1b, and N2b are reset by a reset circuit (not shown) in advance and set at low level (GND) in the initial state, as shown in Fig. 9C. This reset circuit can be realized by, e.g.,

an NMOS transistor.

[0078] In this state, first, the signal PRE of high level (VDD) is supplied to the gate terminals of the transistors Q1a and Q1b, and the signal RE of low level (GND) is supplied to the gate terminals of the transistors Q3a and Q3b. Hence, none of the transistors Q1a, Q1b, Q3a, and Q3b are ON.

15 [0079] In this state, when the signal PRE changes from high level to low level, the transistors Q1a and Q1b are turned on. Since the transistors Q3a and Q3b are kept off, and the signal generation circuits 20 and 52 are stopped, the nodes N2a and N2b are precharged to VDD.

20 [0080] The nodes N1a and N1b are charged until the gate-source voltages of the transistors Q2a and Q2b reach the threshold voltage Vth to turn off the transistors Q2a and Q2b. Since the voltage VDD is applied to the gate terminals of the transistors Q2a and Q2b, the nodes N1a and N1b are precharged to VDD - Vth.

25 [0081] After precharge, when the signal PRE goes high, the transistors Q1a and Q1b are turned off. Simultaneously, the signal RE goes high to turn on the transistors Q3a and Q3b, so the signal generation circuits 20 and 52 change to an operative state. Charges stored at the nodes N1a and N1b are removed from the current sources 21a and 21b to slightly lower the potentials at the node N1a and N1b. The gate-source voltages of the transistors Q2a and Q2b become slightly higher than the threshold voltage Vth to turn on the transistors Q2a and Q2b. With this operation, charges at the nodes N2a and N2b are also removed to start lowering the potentials at the nodes N2a and N2b.

30 [0082] When capacitance Cf > capacitance Cr, the potential at the node N1b is lower than that at the node N1a. Since the ON resistance of the transistor Q2b is lower than that of the transistor Q2a, the potential at the node N2b lowers more quickly than that at the node N2a.

[0083] The potential drop at the node N2b is input to the gate terminal of the NMOS transistor Q2a to increase the ON resistance of the transistor Q2a. For this reason, the potential drop ΔV at the node N2a is suppressed.

35 [0084] Since the potential at the node N2a is input to the gate terminal of the transistor Q2b, the change in ON resistance of the transistor Q2b is small. Consequently, the potential at the node N2b further lowers, and the ON resistance of the transistor Q2a further increases.

[0085] Since the transistors Q2a and Q2b are cross-connected, these operations are augmented to suppress the potential drop ΔV at the node N2a.

40 [0086] Conversely, when capacitance Cf < capacitance Cr, the potential changes at the nodes N2a and N2b are reversed. That is, the potential at the node N2b does not largely change from the initial precharge potential VDD. For this reason, the potential at the node N2a largely lowers, as in the sense unit 1 shown in Fig. 4.

[0087] When the value of the capacitance Cr is set within the above-described range, the gain of the signal amplification circuit 31 can be changed using this threshold value. When a ridge portion of the skin surface of a finger is in contact, a signal (ΔV) of high level is input to the output circuit 40. When a valley portion of the skin surface of a finger is in contact, a signal (ΔV) of low level is input. Hence, the output circuit 40 can clearly determine the ridge and valley portions of the skin surface of a finger.

45 [0088] In the sense unit 1 shown in Fig. 8, a potential drop caused when charges are removed by the leakage current at the node N2a can be canceled by a potential change due to the leakage current at the node N2b. For this reason, any erroneous operation due to the leakage current can be prevented.

50 [0089] In the sense unit 1 shown in Fig. 8, the output circuit 40 is connected to the node N2a. However, the output circuit 40 may be connected to the node N2b. In this case, although the polarity of an output from the output circuit 40 is inverted, the same effect as that when the output circuit 40 is connected to the node N2a can be obtained.

(Third Embodiment)

55 [0090] Fig. 10 shows a sense unit 1 constructing a small capacitance change detection device according to the third embodiment of the present invention. The same reference numerals as in Fig. 8 denote the same parts in Fig. 10, and a detailed description thereof will be omitted.

[0091] The sense unit 1 shown in Fig. 10 is different from the sense unit 1 shown in Fig. 8 in that an output circuit 40a for receiving potential drops ΔV at nodes N2a and N2b as complementary signals is used in place of an output circuit

40.

[0092] The output circuit 40a can be realized using a differential voltage amplification circuit. The output circuit 40a shown in Fig. 10 comprises an NMOS transistor Q4a and resistance Ra, an NMOS transistor Q4b and resistance Rb which have the same characteristics as that of the NMOS transistor Q4a and resistance Ra, and PMOS transistors Q5 and Q6 and NMOS transistors Q7 and Q8, which form a current mirror amplification circuit.

[0093] The operation of the sense unit 1 shown in Fig. 10 is basically the same as that of the sense unit 1 shown in Fig. 8. However, when complementary signals are input to the output circuit 40a, the noise margin for power supply variation and the like can be increased.

10 (Fourth Embodiment)

[0094] Fig. 11 shows a sense unit 1 constructing a small capacitance change detection device according to the fourth embodiment of the present invention. The same reference numerals as in Fig. 8 denote the same parts in Fig. 11, and a detailed description thereof will be omitted.

15 [0095] The sense unit 1 shown in Fig. 11 is different from the sense unit 1 shown in Fig. 8 in that a signal amplification circuit 32 having a switch means connected between nodes N2a and N2b is used in place of a signal amplification circuit 31.

[0096] The switch means is formed from a PMOS transistor Q9 having source and drain terminals connected between the nodes N2a and N2b and gate terminal to which a signal PRE is supplied.

20 [0097] In the sense unit 1 shown in Fig. 8, when the characteristics of the transistors Q1a and Q1b vary, a potential difference may be generated between the nodes N2a and N2b in precharging the nodes N2a and N2b to the power supply voltage VDD. When the nodes N2a and N2b are not precharged to the same potential, the potential drop rates at the nodes N2a and N2b change.

25 [0098] The operation of the sense unit 1 shown in Fig. 11 is basically the same as that of the sense unit 1 shown in Fig. 8. However, in the sense unit 1 shown in Fig. 11, when signal generation circuits 20 and 52 stop, the nodes N2a and N2b can be precharged to the same potential by short-circuiting the nodes N2a and N2b by the transistor Q9. In addition, during signal detection, i.e., when the signal generation circuits 20 and 52 are operating, the nodes N2a and N2b are opened by the transistor Q9.

30 [0099] With this arrangement, the changes in potential drop rates at the nodes N2a and N2b can be suppressed, and the surface shape detection accuracy can be prevented from lowering.

[0100] In the sense unit 1 shown in Fig. 11, an output circuit 40 is connected to the node N2a. However, the output circuit 40 may be connected to the node N2b. In this case, although the polarity of an output from the output circuit 40 is inverted, the same effect as that when the output circuit 40 is connected to the node N2a can be obtained.

35 (Fifth Embodiment)

[0101] Fig. 12 shows a sense unit 1 constructing a small capacitance change detection device according to the fifth embodiment of the present invention. The same reference numerals as in Figs. 10 and 11 denote the same parts in Fig. 12, and a detailed description thereof will be omitted.

40 [0102] The sense unit 1 shown in Fig. 12 is different from the sense unit 1 shown in Fig. 10 in that a signal amplification circuit 32 shown in Fig. 11 is used in place of a signal amplification circuit 31.

[0103] In the sense unit 1 shown in Fig. 12, when nodes N2a and N2b are precharged to a power supply voltage VDD, the potential difference between the nodes N2a and N2b due to variations in characteristics of transistors Q1a and Q1b can be eliminated. For this reason, unlike the sense unit 1 shown in Fig. 10, an offset voltage generated by complementary inputs to the differential amplification circuit due to this potential difference, or a decrease in detection accuracy due to changes in potential drop speeds at the nodes N2a and N2b can be prevented.

45 (Sixth Embodiment)

50 [0104] Fig. 13 shows a sense unit 1 constructing a small capacitance change detection device according to the sixth embodiment of the present invention. The same reference numerals as in Fig. 4 denote the same parts in Fig. 13, and a detailed description thereof will be omitted.

[0105] The sense unit 1 shown in Fig. 13 is constructed using transistors Q1c, Q2c, Q3c, and Q4c with polarities different from those of the transistors Q1a to Q1a in Fig. 4. Referring to Fig. 13, the transistor Q1c is an NMOS transistor, and the transistors Q2c to Q4c are PMOS transistors. Signals PRE and RE obtained by inverting the polarities of signals PRE and RE are supplied to the transistors Q1c and Q3c. A power supply voltage VDD is applied to the input side of a current source 21a. The source terminal of the transistor Q1c is connected to ground. Reference symbols Cp1c and Cp2c denote parasitic capacitances.

[0106] Figs. 14A to 14C explain the operation of the sense unit 1 shown in Fig. 13. The operation of the sense unit 1 is the same as that of the sense unit 1 shown in Fig. 4 except that the polarities of signals are inverted, and the direction in which the signal (ΔV) changes is reversed, and the same effect as that of the sense unit 1 shown in Fig. 4 can be obtained. Referring to Fig. 13, the potentials at the nodes N1c and N2c are reset by a reset circuit (not shown) in advance and set at high level (VDD) in the initial state, as shown in Fig. 14C. This reset circuit can be realized by, e.g., a PMOS transistor.

[0107] A potential rise ΔV at the node N2c after a period Δt elapses is given by $VG + Vth + I\Delta t/(Cf + Cp1c)$.

[0108] For the sense units 1 shown in Figs. 8 and 10 to 12 as well, the same effect as described above can be obtained by using transistors with polarities different from those of the transistors Q1b to Q4b and Q9.

10 (Seventh Embodiment)

[0109] Figs. 15A to 15C show a small capacitance change detection device according to the seventh embodiment of the present invention. The same reference numerals as in Fig. 2 denote the same parts in Figs. 15A to 15C, and a detailed description thereof will be omitted.

[0110] In the small capacitance change detection device shown in Fig. 2, a signal generation circuit 20, signal amplification circuit 30, and output circuit 40 are arranged for each detection element 10 to form a sense unit 1. A plurality of sense units 1 are two-dimensionally arrayed to form a sensor array 2. In this case, detection can be parallelly processed, and detection processing at high speed is possible.

[0111] Unlike this device, at least one of the signal generation circuit 20, signal amplification circuit 30, and output circuit 40 may be shared by a plurality of detection elements 10.

[0112] To share the signal generation circuit 20, one signal generation circuit 20 is selectively connected to one of the plurality of detection elements 10 by a switch SW2, as shown in Fig. 15A.

[0113] To share the signal amplification circuit 30, one signal amplification circuit 30 is selectively connected to one of the plurality of signal generation circuits 20 and one of the plurality of output circuits 40 by switches SW3 and SW4, as shown in Fig. 15B. The switches SW3 and SW4 operate in synchronism with each other.

[0114] To share the output circuit 40, one output circuit 40 is selectively connected to one of the plurality of signal amplification circuits 30 by a switch SW5, as shown in Fig. 15C.

[0115] When at least one of the signal generation circuit 20, signal amplification circuit 30, and output circuit 40 is shared by the plurality of detection elements 10, the circuit scale or operating current can be reduced.

[0116] When the plurality of detection elements 10 arranged close to each other share the signal generation circuit 20, signal amplification circuit 30, and output circuit 40, the influence of parasitic elements formed in the manufacturing process becomes small.

[0117] In the sense units 1 shown in Figs. 8 and 10 to 12 as well, at least one of the signal generation circuit 20, signal amplification circuit 31 or 32, and output circuit 40 or 42 can be shared by a plurality of detection elements 10.

35 (Eighth Embodiment)

[0118] Fig. 16 shows a small capacitance change detection device according to the eighth embodiment of the present invention. The same reference numerals as in Fig. 7 denote the same parts in Fig. 16, and a detailed description thereof will be omitted.

[0119] A reference signal generation circuit 50 shown in Fig. 7 can be shared by a plurality of signal amplification circuits 31. In this case, as shown in Fig. 16, one signal amplification circuit 31 is selectively connected to one of the plurality of signal amplification circuits 31 by switches SW6 and SW7. With this arrangement, the circuit scale or operating current can be reduced.

[0120] In the sense units 1 shown in Figs. 10 to 12 as well, the reference signal generation circuit 50 can be shared by a plurality of signal amplification circuits 31 or 32.

50 (Ninth Embodiment)

[0121] Figs. 17A and 17B show other implementations of a signal amplification circuit 30 shown in Fig. 2.

[0122] As shown in Fig. 17A, the signal amplification circuit 30 can be realized by an inverting amplifier 33 for amplifying a voltage signal. Reference symbol G denotes a voltage gain.

[0123] As shown in Fig. 17B, the signal amplification circuit 30 can also be realized by a current mirror circuit 34 for amplifying a current signal. Reference symbol n denotes a current gain. Fig. 19B shows the current mirror circuit 34 for amplifying a current using a gate width W of PMOS transistors Q10 and Q11. However, the present invention is not limited to this.

[0124] A differential signal amplification circuit 31 shown in Fig. 7 can also be realized by a current mirror circuit.

[0125] The present invention can be applied to recognize not only a human fingerprint but also a surface shape having a fine three-dimensional pattern of, e.g., nose of an animal.

(10th Embodiment)

[0126] Figs. 18A and 18B shows a small capacitance change detection device according to the 10th embodiment of the present invention. Fig. 18A shows the main part of a surface shape recognition sensor constructing the device. Fig. 18B shows an equivalent circuit.

[0127] This surface shape recognition sensor comprises a detection element 10 shown in Fig. 2 and a reference element 51 of a reference signal generation circuit 50 shown in Fig. 7. As shown in Fig. 18A, a matrix-like support member 103 consisting of a conductive material is formed on a semiconductor substrate 101 via an insulating layer 102. A lower electrode 104 is formed on the insulating layer 102 at the center of each square (cell) surrounded by the support member 103 to be separated from the support member 103. An upper electrode 105 is formed on the support member 103.

[0128] The upper electrode 105 is separated from the lower electrode 104 by a predetermined distance. The lower electrode 104 and upper electrode 105 form a capacitance Cf. In this surface shape recognition sensor, a protective film 106 having a projecting portion 106a is formed on the upper electrode 105. The projecting portion 106a is formed in an area above the lower electrode 104.

[0129] A reference electrode 104a is formed on the insulating layer 102 to surround the lower electrode 104 while being separated from the lower electrode 104 and support member 103.

[0130] The difference between the capacitance Cf between the upper electrode 105 and lower electrode 104 and a capacitance Cr between the upper electrode 105 and reference electrode 104a is detected by a sensor circuit 110. The equivalent circuit of the capacitances Cf and Cr and sensor circuit 110 is shown in Fig. 18B.

[0131] As shown in Fig. 19, the support member 103 is formed in a matrix. The lower electrode 104 and reference electrode 104a are formed at the central portion of each cell to form a matrix. That is, the surface shape recognition sensor is formed from a plurality of sensor elements each having the lower electrode 104, reference electrode 104a, and upper electrode 105 formed on these electrodes.

[0132] A sensor circuit 110 is prepared in correspondence with one lower electrode 104 and one reference electrode 104a. A sensor circuit 110 may be prepared in correspondence with a plurality of lower electrodes 104 and reference electrodes 104a. The sensor circuit 110 may be integrated under the insulating layer 102 on the semiconductor substrate 101 or formed in an area of the semiconductor substrate 101, where no sensor is arranged. The sensor circuit 110 may be prepared outside the semiconductor substrate 101. Note that an interconnection structure for connecting the electrodes to the sensor circuit is formed on the semiconductor substrate 101.

[0133] The operation of the surface shape recognition sensor according to the 10th embodiment will be described next.

[0134] As shown in Fig. 20, when the projecting portion 106a comes into contact with an object, the protective film 106 deforms and simultaneously the upper electrode 105 also deforms. As a consequence, the distance between the lower electrode 104 and upper electrode 105 changes to change the capacitance Cf therebetween. At the same time, the distance between the reference electrode 104a and upper electrode 105 changes to change the capacitance Cr therebetween.

[0135] In the above-described sense unit 1 shown in Fig. 8, since the detection element 10 is formed from the capacitance Cf, and the reference element 51 in the reference signal generation circuit 50 is formed from the capacitance Cr, a signal based on the capacitance Cr is output from the reference signal generation circuit 50 as a reference signal.

[0136] As is apparent from Fig. 20, the change amount of the upper electrode 105 is small near the support member 103. That is, the change in distance between the reference electrode 104a and upper electrode 105 is smaller than that between the lower electrode 104 and upper electrode 105.

[0137] Hence, the capacitances Cf and Cr change as shown in Fig. 21 with respect to the amount of movement a portion (central portion of the upper electrode) of the upper electrode 105 under the projecting portion 106a in the direction of lower electrode 104 when the projecting portion 106a comes into contact with an object. In this case, the initial values of the capacitances Cf and Cr can be made equal by setting the surface area of the reference electrode 104a to be equal to that of the lower electrode 104, as shown in Fig. 21.

[0138] The relationship between the change in capacitance Cf and the change in capacitance Cr, which is shown in Fig. 21, does not depend on the height (thickness) of the support member 103. When the difference is detected by the sensor circuit 110, a constant detection result can be obtained even when the height of the support member 103 changes. In other words, when the magnitude of the capacitance Cf is detected using the capacitance Cr as a reference, the change in the absolute value does not affect the detection result by the sensor circuit 110.

[0139] The difference between capacitance changes is detected by the sensor circuit 110 as an electrical signal. When the detected value exceeds the threshold value, it can be determined that the projecting portion 106a is deformed and consequently, the three-dimensional pattern of the object can be detected.

[0140] The skin surface at a finger tip is formed by ridge and valley portions. When a finger is brought into contact with the protective film 106, the deformation amount of the projecting portion 106a changes between a case wherein the projecting portion 106a is in contact with a ridge portion of the skin surface of a finger and a case wherein the projecting portion 106a is in contact with a valley portion. This difference in deformation amount is detected as the difference in capacitance change.

[0141] Hence, when the distribution of detection results different in units of a plurality of sensor elements is determined and detected using the threshold value, the detection results represent the shape of ridge portions of the skin surface of a finger. That is, with the capacitive surface shape recognition sensor of the 10th embodiment, the fine ridge and valley portions of the skin surface can be detected.

[0142] According to the surface shape recognition sensor of the 10th embodiment, even when the height of the support member has a manufacturing variation, the variation does not adversely affect the detection result of the sensor circuit 110, so any recognition error of the object shape can be prevented.

[0143] Since variations are rarely generated between detection results of the plurality of sensor elements, the finger-print pattern can be accurately detected.

[0144] According to the above 10th embodiment, in one sensor element, the reference electrode has a ring-like integral structure to surround the lower electrode. However, the present invention is not limited to this. The same effect as described above can be obtained even when a plurality of divided reference electrodes are arranged around the lower electrode.

[0145] The same effect as in the 10th embodiment can be obtained even when a rectangular reference electrode is formed at a portion between the support member and lower electrode in one sensor element. In this case, a plurality of reference electrodes may be prepared in correspondence with one lower electrode, and a plurality of capacitances between the upper electrode and the plurality of reference electrodes may be compared with the capacitance between the upper electrode and lower electrode.

[0146] In the 10th embodiment, the protective film having a projecting portion is formed on the upper electrode. However, the present invention is not limited to this. Formation of a flat protective film on the upper electrode suffices. When metal material having corrosion resistance is used for the upper electrode, no protective film need be formed on the upper electrode.

(11th Embodiment)

[0147] Fig. 22 shows a small capacitance change detection device according to the 11th embodiment of the present invention. Fig. 22 shows another arrangement of a signal generation circuit 20 shown in Fig. 2.

[0148] The signal generation circuit shown in Fig. 22 removes charges by charging/discharging the capacitance and is similar to the first signal generation circuit 22 shown in Fig. 6 in use of charge/discharge of the capacitance. However, unlike the first signal generation circuit 22 shown in Fig. 6, the amount of charges to be removed is controlled by a capacitance C_s and a driving voltage V_s . More specifically, the amount of charges to be removed is controlled by setting the driving voltage V_s shown in Fig. 22 at the power supply voltage level (VDD) or ground level (GND) through a switch SW11. The controllability of the capacitance C_s is higher than that of, e.g., the current value of a current source 21a shown in Fig. 8. The voltage can be easily and accurately controlled using the above-described power supply voltage, as compared to time control.

[0149] An optimum value for the capacitance value setting method will be described next.

[0150] As shown in Figs. 23A to 23C, a potential P is set at high level to close the switch for precharge. After this, the potential P is set at low level to open the switch, and charges are removed using the driving capacitance C_s to generate an input signal to the side of a detection circuit 120 formed from the signal generation circuit and output circuit. Let V_p be the precharge potential, C_f be the detection capacitance, and C_p be the parasitic capacitance. A change amount ΔV of the input signal is given by

$$\Delta V = \Delta V_s / \{1 + (C_f + C_p)/C_s\} \quad (2)$$

[0151] A dynamic range ΔV_i of this signal change amount is given by

$$\begin{aligned} \Delta V_i &= \Delta V_{MAX} - \Delta V_{MIN} \\ &= \Delta V_s / \{1 + (C_{fv} + C_p)/C_s\} - \Delta V_s / \{1 + (C_{fr} + C_p)/C_s\} \end{aligned} \quad (3)$$

[0152] where C_{fv} is the capacitance of a valley portion of the skin surface of a finger, and C_{fr} is the capacitance of a ridge portion of the skin surface of a finger. The dynamic range ΔV_i is preferably as large as possible because it corresponds to an input signal to the detection circuit 120. Fig. 24 shows the relationship between the dynamic range ΔV_i and capacitance C_s when $C_p = 50 \text{ fF}$, $C_{fv} = 10 \text{ fF}$, $C_{fr} = 100 \text{ fF}$, and $\Delta V_s = 2.7 \text{ V}$.

[0151] Referring to Fig. 24, there is a capacitance C_s at which the dynamic range ΔV_i is maximized. The capacitance C_s is about 95 fF. From the above equations, the dynamic range ΔV_i is maximized when

$$C_s = \{(C_{fv} + C_p)(C_{fr} + C_p)\}^{1/2} \quad (4)$$

The capacitance C_s is selected to satisfy this condition. The size of a sensor electrode is limited on the basis of the fingerprint pattern and sensitivity of a sensor circuit and set to be about 20 to 100 μm square. At this time, the capacitance C_{fr} is about 20 to 350 fF, the capacitance C_{fv} is about 5 fF or less, and the parasitic capacitance C_p is about 10 to 170 fF. The capacitance C_{fv} is small and therefore may be fixed at 5 fF. Fig. 25 shows the optimum value of the capacitance C_s when the capacitances C_{fr} and C_p are changed.

[0152] In actual manufacturing, it can be considered that $C_p = C_{fv}/3$ and $C_{fr} = C_{fv}/20$. In this case, the optimum value of the capacitance C_s is about 0.7 C_{fv} . This relationship is shown in Fig. 26. The optimum value of the capacitance C_s is about 0.7 times the capacitance C_{fv} and falls within the range of about 14 to 245 fF on the basis of the range of the capacitance C_{fv} .

[0153] In the 11th embodiment of the present invention, charge removal is done using not a current source but charge/discharge of the capacitance. For this reason, it is unnecessary to accurately control the current amounts of internal current sources of a number of sensor cells and the charge removal time. Hence, the sensing accuracy of the detection circuit can be improved with a simple arrangement.

20 (12th Embodiment)

[0154] Fig. 27 shows a small capacitance change detection device according to the 12th embodiment of the present invention. This device has a voltage-time conversion circuit 141 as an output circuit 40 shown in Fig. 2.

[0155] Fig. 28 shows the circuit arrangement of the small capacitance change detection device shown in Fig. 27. This arrangement is different from the circuit shown in Fig. 4 in the voltage-time conversion circuit 141 is arranged in place of the output circuit 40.

[0156] As shown in Fig. 28, the voltage-time conversion circuit 141 comprises a variable current source 43 for converting an input signal ΔV_o into a current signal, load capacitance CL charged with the current from the variable current source 43, threshold circuit 42 which receives the potential at a node N3a and changes the signal to be output on the basis of a certain threshold voltage, and reset circuit 44 for resetting the potential at the node N3a.

[0157] Figs. 29A to 29D show operations of various sections of the small capacitance change detection device shown in Fig. 28. The operation of the small capacitance change detection device will be described with reference to these timing charts.

[0158] When a voltage signal ΔV_i corresponding to a capacitance C_f of a detection element 10 is output (Fig. 29A), the voltage signal ΔV_i is amplified to ΔV_o by a signal amplification circuit 30 and output to the voltage-time conversion circuit 141 (Fig. 29B). A current corresponding to the input signal ΔV_o flows from the variable current source 43 of the voltage-time conversion circuit 141 to charge the load capacitance CL . With this operation, the potential at the node N3a of the voltage-time conversion circuit 141 rises (Fig. 29C).

[0159] When the potential at the node N3a exceeds a threshold voltage V_t of the threshold circuit 42, the output voltage from an output signal OUT changes (Fig. 29D). The signal polarity is merely an example and is not limited to this. In this case, since the current amount of the variable current source 43 changes depending on the magnitude of the input signal ΔV_o , the manner in which the potential increases at the node N3a changes. A time T_s until the output signal changes is given by

$$T_s = CL \cdot V_t/gm \Delta V_o \quad (5)$$

where gm is the transconductance of the variable current source 43.

[0160] When the capacitance C_f is about 100 fF or less, the input signal ΔV_o is approximately in proportion to the magnitude of the capacitance C_f , and the time T_s is in proportion to a distance d between the electrode of the detection element 10 and the skin surface of a finger. Hence, the signal corresponding to the distance from the skin surface of a finger can be represented by the time. The output dynamic range can be increased without being limited by the power supply voltage or linear region of an analog amplifier. The variable current source 43 can be realized by, e.g., a PMOS transistor. The threshold circuit 42 can be realized using an inverter circuit or a circuit such as a Schmidt trigger circuit having hysteresis in its threshold value. When a circuit such as a Schmidt trigger circuit having hysteresis in its threshold value is used, the output signal from the threshold circuit 42 can be prevented from changing due to a voltage variation by noise even when the potential at the node N3a moderately changes. When the polarities of signals or power supply are inverted, the polarities of MOS transistors are inverted. This arrangement is not illustrated because it is readily understood by those skilled in the art. For example, as the variable current source 43, an NMOS transistor can be

used.

(13th Embodiment)

5 [0161] Fig. 30 shows a small capacitance change detection device according to the 13th embodiment of the present invention. An output circuit 40 shown in Fig. 2 is built by an output circuit 140 and bias adjusting circuit 160. In the device shown in Fig. 30, the output circuit 140 can be adjusted by the bias adjusting circuit 160.

10 [0162] Referring to Fig. 31, the output circuit 140 has a variable threshold circuit 45, and the threshold voltage of the variable threshold circuit 45 is adjusted by a threshold adjusting circuit 161. The threshold adjusting circuit 161 is a specific example of the bias adjusting circuit 160 shown in Fig. 30. The variable threshold circuit 45 in the output circuit 140 can be realized by a Schmidt trigger circuit as shown in Fig. 32. When such a circuit is used as the variable threshold circuit 45, and nodes N4 of sense units 1 shown in Fig. 1 are connected to each other, the sense units function as the threshold adjusting circuits 161. With this arrangement, the threshold voltage of the variable threshold circuit 45 in the output circuit 140 changes depending on the states of output signals from the sense units 1. For example, assume that a voltage signal from an output circuit at a valley portion of the skin surface of a finger is larger than that from an output circuit at a ridge portion of skin surface of the finger. The contrast of the ridge and valley portions of the skin surface of the finger can be enhanced by adjusting the threshold voltage of the variable threshold circuit 45 such that the signal from the output circuit at the ridge portion is made smaller than the signal from the output circuit at the valley portion.

15 [0163] In the same circuit arrangement as described above, an analog amplifier can be used as the variable threshold circuit 45, and the threshold adjusting circuit 161 can be operated as the bias adjusting circuit of the analog amplifier. The contrast can be enhanced by adjusting the bias of the analog amplifier in accordance with the output signal states of the sense units. Hence, according to the 13th embodiment, the function of enhancing the contrast of the surface shape can be realized.

25 (14th Embodiment)

25 [0164] Fig. 33 shows a small capacitance change detection device according to the 14th embodiment of the present invention. An output circuit 40 shown in Fig. 20 is built by a voltage-time conversion circuit 141 and bias adjusting circuit 160.

30 [0165] In the 14th embodiment, the voltage-time conversion circuit 141 is used as the output circuit 40, and the voltage-time conversion circuit 141 is adjusted by the bias adjusting circuit 160.

35 [0166] Referring to Fig. 34, the voltage-time conversion circuit 141 shown in Fig. 33 has a variable threshold circuit 45, and the threshold voltage of the variable threshold circuit 45 can be adjusted by a threshold adjusting circuit 161. The threshold adjusting circuit 161 shown in Fig. 34 is a specific example of the bias adjusting circuit 160 shown in Fig. 33. The variable threshold circuit 45 can be realized by a Schmidt trigger circuit as shown in Fig. 32. When such a circuit is used as the variable threshold circuit, and nodes N4 of sense units 1 are connected to each other, the sense units function as threshold adjusting circuits. With this arrangement, the threshold voltage of the variable threshold circuit 45 in the voltage-time conversion circuit 141 changes depending on the states of output signals from the sense units 1.

40 [0167] For example, assume that an output signal T_s from a voltage-time conversion circuit at a valley portion of the skin surface of a finger is larger than the output signal T_s from a voltage-time conversion circuit at a ridge portion of skin surface of the finger. The contrast of the ridge and valley portions of the skin surface of the finger can be enhanced by adjusting the threshold voltage of the variable threshold circuit such that the signal from the voltage-time conversion circuit at the valley portion is made larger than the signal from the voltage-time conversion circuit at the ridge portion, i.e., the threshold voltage becomes high. Hence, according to the 14th embodiment, the function of increasing the output dynamic range and enhancing the contrast of the surface shape can be realized.

45 (15th Embodiment)

50 [0168] Fig. 35 shows a small capacitance change detection device according to the 15th embodiment of the present invention. An output circuit 40 shown in Fig. 7 is formed from a voltage-time conversion circuit 141. When the output circuit 40 is constructed as a voltage-time conversion circuit, the same effect as in the above-described 12th embodiment can be obtained.

(16th Embodiment)

55 [0169] Fig. 36 shows a small capacitance change detection device according to the 16th embodiment of the present invention. An output circuit 40 shown in Fig. 7 is formed from an output circuit 140 shown in Fig. 30, and the output circuit 140 is adjusted by a bias adjusting circuit 160. With this arrangement, the same effect as in the above-described

13th embodiment can be obtained.

(17th Embodiment)

5 [0170] Fig. 37 shows a small capacitance change detection device according to the 17th embodiment of the present invention. An output circuit 40 shown in Fig. 7 is formed from a voltage-time conversion circuit 141 shown in Fig. 33, and the voltage-time conversion circuit 141 is adjusted by a bias adjusting circuit 160. With this arrangement, the same effect as in the above-described 14th embodiment can be obtained.

10 [0171] As described above, in the 12th to 17th embodiments, the output dynamic range of the device can be increased by converting the output signal into a signal in the direction of time. In addition, when the bias of the internal circuit of the output circuit is adjusted, the contrast can be enhanced. Furthermore, by combining these circuits, a wide dynamic range and high contrast can be simultaneously realized. When this device is applied to a fingerprint sensor using the LSI manufacturing technology, a highly accurate fingerprint image can be obtained even by an A/D converter with low resolving power because of the dynamic range increase and contrast enhancement function. Especially, application of this device in a low-voltage operative state allows obtaining a highly accurate fingerprint image.

(18th Embodiment)

20 [0172] Fig. 38 shows the 18th embodiment of the present invention. Fig. 38 shows the circuit arrangement of a variable threshold circuit 45a arranged in an output circuit 140 shown in Fig. 31 as a variable threshold circuit shown in Fig. 32. The logic threshold value of this variable threshold circuit 45a can be adjusted or controlled after manufacturing.

[0173] The variable threshold circuit 45a shown in Fig. 38 or each of variable threshold circuits to be described later is constructed by a Schmidt trigger circuit.

25 [0174] Referring to Fig. 38, reference symbol Q11 denotes a PMOS transistor; and Q12 and Q13, NMOS transistors. Reference numeral 46 denotes an inverter gate. Reference symbol VDD denotes a power supply voltage; and N4 and N5, nodes. The conductivity of an active element 47 changes in accordance with the level of a signal indicated by an arrow A. The active element 47 is turned off when an output signal OUT goes high. In this case, the active element 47 can be realized by, e.g., a PMOS transistor.

30 [0175] In this variable threshold circuit 45a, the conductivity of the active element 47 is controlled by the output signal OUT. The variable threshold circuit 45a has the above-described elements. This is different from the conventional circuit in that the potential at the node N4 for connecting the active element 47 can be applied from an external element of the variable threshold circuit 45a. The potential at the node N4 is adjusted by a threshold adjusting circuit 161 shown in Fig. 31.

35 [0176] Referring to Fig. 38, when the potential at the node N4 is increased/decreased, the potential at the node N5 also increases/decreases accordingly. For this reason, by controlling the potential at the node N4, the logic threshold value for changing an input signal IN from low level to high level can be adjusted.

[0177] As shown in Fig. 39, when the nodes N4 of a plurality of variable threshold circuits 45a₁ to 45a_n are connected, and a load element 48 is inserted between the nodes N4 and the power supply potential VDD, the logic threshold value can be dynamically changed in accordance with the input waveform.

40 [0178] The load element 48 can be realized by, e.g., a resistive element or a MOS transistor biased by a gate electrode potential. In Fig. 39, n variable threshold circuits 45a₁ to 45a_n are connected. Input signals IN1, IN2, ..., INn and output signals OUT1, OUT2, ..., OUTn correspond to the variable threshold circuits 45a₁ to 45a_n, respectively.

45 [0179] Referring to Fig. 39, a case wherein the potential changes of the input signals have different slopes will be considered. For the descriptive convenience, assume that the input signal IN1 has the steepest slope, the input signal IN2 has a relatively moderate slope, and the input INn has the most moderate slope.

[0180] Fig. 40 shows operation waveforms when such input waveforms are input to the circuit as shown in Fig. 39.

[0181] Referring to Fig. 40, when all the input signals are at low level, all the variable threshold circuits 45a₁ to 45a_n have a logic threshold value Vta. When the input signals begin to change, the potential of the input signal IN1 reaches the logic threshold value Vta first, so the output signal OUT1 output from the variable threshold circuit 45a₁ first goes high. As a result, the active element 47 in the variable threshold circuit 45a₁ controlled by the output signal OUT1 is turned off, and the potential at the node N4 shown in Fig. 39 slightly rises. Hence, the logic threshold value of all the variable threshold circuits 45a₁ to 45a_n becomes slightly higher than Vta.

50 [0182] When the input signal IN2 exceeds the logic threshold value after change, the same operation as described above is performed. Finally, when the input signal INn exceeds the logic threshold value, the logic threshold value has increased to Vtb. Hence, the output timing of the output signal OUTn can be delayed as compared to the conventional output signal.

55 [0183] As is apparent from the above description, the logic threshold value of the variable threshold circuit 45a dynamically changes in accordance with the operation of the remaining variable threshold circuits. This effect can also be

obtained for input waveforms which are the same but have different input timings. Hence, when the variable threshold circuit 45a is used, the logic threshold value can be changed in accordance with the input waveform.

5 (19th Embodiment)

[0184] Fig. 41 shows the 19th embodiment of the present invention.

[0185] The basic arrangement is the same as in the 18th embodiment. However, a variable threshold circuit 45b is different from the 18th embodiment in that a load element 49 is connected between a node N4 and power supply voltage VDD in the variable threshold circuit 45b. The load element 49 can be realized by, e.g., a resistive element or a 10 MOS transistor biased by a gate electrode potential. With this arrangement, the initial value of the potential at the node N4 can be set on the basis of the ON resistance ratio of an active element 47 to a transistor Q13. After this, by changing the potential at the node N4, the logic threshold value of the variable threshold circuit 45b is adjusted as in the 18th embodiment.

[0186] As shown in Fig. 42, when the nodes N4 of a plurality of variable threshold circuits 45b₁ to 45b_n are connected, 15 the logic threshold value can be dynamically changed in accordance with the input waveform. The operation principle and effect are the same as in the 18th embodiment shown in Fig. 39.

(20th Embodiment)

20 [0187] Fig. 43 shows the 20th embodiment of the present invention.

[0188] A variable threshold circuit 45c of the 20th embodiment shown in Fig. 43 is different from the variable threshold circuit 45b of the 19th embodiment shown in Fig. 41 in that the ON resistance of a load element 49 is controlled by the potential at a node N4. In the 20th embodiment, the ON resistance is changed by changing the potential at the node N4, and consequently, the logic threshold value of the variable threshold circuit 45c can be adjusted.

25 (21st Embodiment)

[0189] Fig. 44 shows the 21st embodiment of the present invention.

[0190] For a variable threshold circuit 45d of the 21st embodiment shown in Fig. 44, the polarity of a MOS transistor 30 of the variable threshold circuit 45a of the 18th embodiment shown in Fig. 38 is inverted (Q12 → Q15), a power supply potential VDD is replaced with ground GND, and a node N6 is arranged in place of the node N4.

[0191] In the variable threshold circuit 45d of the 21st embodiment, the logic threshold value can be adjusted by controlling the potential at the node N6 when the input waveform changes from high level to low level.

35 (22nd embodiment)

[0192] In the 22nd embodiment of the present invention, the polarity of the MOS transistor Q12 in the variable threshold circuit 45b of the 19th embodiment shown in Fig. 41 is inverted, a power supply potential VDD is replaced with ground GND, and a node N6 is arranged in place of the node N4, as in conversion from Fig. 38 to Fig. 44. The 22nd embodiment is not illustrated because it can be easily estimated from the figure (Fig. 41) of the 19th embodiment.

[0193] In the variable threshold circuit of the 22nd embodiment, the logic threshold value can be adjusted by controlling the potential at the node N6 when the input waveform changes from high level to low level, as in the variable threshold circuit 45d of the 21st embodiment shown in Fig. 44.

45 (23rd Embodiment)

[0194] In the 23rd embodiment of the present invention, the polarity of the MOS transistor Q12 in the variable threshold circuit 45c of the 20th embodiment shown in Fig. 43 is inverted, a power supply potential VDD is replaced with ground GND, and a node N6 is arranged in place of the node N4, as in conversion from Fig. 38 to Fig. 44. The 23rd embodiment is not illustrated because it can be easily estimated from the figure (Fig. 43) of the 20th embodiment.

[0195] In the variable threshold circuit of the 23rd embodiment, the logic threshold value can be adjusted by controlling the potential at the node N6 when the input waveform changes from high level to low level, as in the variable threshold circuit 45d of the 21st embodiment shown in Fig. 44.

55 (24th embodiment)

[0196] Fig. 45 shows the 24th embodiment of the present invention. A variable threshold circuit 45e of the 24th embodiment is formed by combining the variable threshold circuit 45a of the 18th embodiment shown in Fig. 38 and var-

iable threshold circuit 45d of the 21st embodiment shown in Fig. 44 into one circuit.

[0197] In the variable threshold circuit 45e of the 24th embodiment, the logic threshold value can be adjusted when the input waveform changes from low level to high level, as in the variable threshold circuit 45a of the 18th embodiment shown in Fig. 38. In addition, when the input waveform changes from high level to low level, the logic threshold value can be adjusted, as in the variable threshold circuit 45d of the 21st embodiment shown in Fig. 44.

(25th embodiment)

[0198] In the 25th embodiment of the present invention, the variable threshold circuit 45b of the 19th embodiment shown in Fig. 41 and the above-described 22nd embodiment are combined into one circuit. The 25th embodiment is not illustrated because it can be easily estimated from the figure (Fig. 41) of the 19th embodiment and the above-described 22nd embodiment.

[0199] In the variable threshold circuit of the 25th embodiment, when the input waveform changes from low level to high level, the logic threshold value can be adjusted, as in the variable threshold circuit 45b of the 19th embodiment shown in Fig. 41. When the input waveform changes from high level to low level, the logic threshold value can be adjusted, as in the 22nd embodiment.

(26th embodiment)

[0200] In the 26th embodiment of the present invention, the variable threshold circuit 45c of the 20th embodiment shown in Fig. 43 and the variable threshold circuit of the 23rd embodiment are combined into one circuit. The 26th embodiment is not illustrated because it can be easily estimated from the figure (Fig. 43) of the 20th embodiment and the above-described 23rd embodiment.

[0201] In the variable threshold circuit of the 26th embodiment, when the input waveform changes from low level to high level, the logic threshold value can be adjusted, as in the 20th embodiment shown in Fig. 43. When the input waveform changes from high level to low level, the logic threshold value can be adjusted, as in the 23rd embodiment.

[0202] In the above variable threshold circuits, a signal having the same polarity as that of an input signal is output. When one inverter circuit is added to the output side, a variable threshold circuit for outputting the inverted signal of the input signal IN can be formed. When the inverter gate 46 is omitted, or the inverter gate 46 is replaced with a buffer circuit, a variable threshold circuit for outputting the inverted signal of the input signal IN can be obtained. In this case, the active element 47 is turned off when the output signal OUT goes low. The active element 47 can be realized by, e.g., an NMOS transistor.

[0203] As described above, in the variable threshold circuits of the 18th to 26th embodiments, the logic threshold value can be changed after manufacturing the circuit. When the input level deviates from the design value due to the manufacturing variation in the circuit, the input level can be adjusted by changing the logic threshold value. In addition, when input waveforms have different slopes or different input timings, the waveforms can be shaped while dynamically changing the logic threshold value. As a consequence, when the input waveform changes due to the manufacturing variation in the circuit or in accordance with the operation condition, a desired waveform shaping output can be obtained.

[0204] When the nodes N4 or N6 of the variable threshold circuits of each of the 18th to 26th embodiments are connected to connect the sense units 1 shown in Fig. 1 to each other, each sense unit functions as a variable threshold circuit. When the voltage value from the output circuit at the valley portion of the skin surface of a finger is larger than that at a ridge portion, the threshold voltage changes such that the voltage signal from the output circuit at the ridge portion is made smaller by the voltage signal from the output circuit at the valley portion, and the contrast of the ridge and valley portions of the skin surface of a finger can be increased.

(27th Embodiment)

[0205] Fig. 46 shows a small capacitance change detection device according to the 27th embodiment of the present invention. Fig. 46 shows a section of one sensor element (detection element 10 shown in Fig. 2) in a sensor array two-dimensionally arrayed on a semiconductor substrate and the arrangement of a signal generation circuit 20 shown in Fig. 2.

[0206] Referring to Fig. 46, reference numeral 104 denotes a lower electrode; 107, a metal film; 103, a support member; 105, an upper electrode; 101, a semiconductor substrate; 106, a protective film; and 120, a detection circuit. Reference symbol SW10 denotes a switch. The sensor elements are isolated by the support member 103. Referring to Fig. 46, a capacitance Cf is formed between the upper electrode 105 and lower electrode 104. The capacitance Cf reflects the three-dimensional pattern of the surface shape of a measurement object such as a finger 3 in Fig. 1, which is placed on the protective film 106. Reference symbol Cp denotes a parasitic capacitance; and Vp, an external potential applied to a node N1 (corresponding to a node N1a in Fig. 4) in Fig. 46. Reference symbol P denotes a control signal of the

switch SW10. The switch SW10 can be realized by, e.g., a MOS transistor. The detection circuit 120 corresponds to a signal amplification circuit 30 and output circuit 40 shown in Fig. 2. Reference numeral 130 denotes a control means.

[0207] The operation of the small capacitance change detection device shown in Fig. 46 will be described with reference to the timing charts shown in Figs. 47A to 47C.

5 [0208] At time ① in Fig. 47B, the control means 130 sets a voltage Vs at a node N2 to a constant potential and applies the voltage Vs to the upper electrode 105 through the metal film 107 and support member 103 as a conductive member. Next, at time ② in Fig. 47A, the control means 130 sets the control signal P at high level to turn on the switch SW10 to precharge the node N1 shown in Fig. 46 with the external voltage Vp, thereby charging the capacitance Cf. After the node N1 is precharged, at time ③ in Fig. 47A, the control means 130 sets the control signal P at low level to turn off the switch SW10 and also changes the voltage Vs at the node N2 by ΔV s from the constant potential, as shown in Fig. 47B.

10 [0209] When the change amount of the voltage Vs is ΔV s, the potential at the node N1 changes due to capacitive coupling by the capacitance Cf, so the change amount of the potential at the node N1 is represented by

15
$$Cf/(Cf + Cp) * \Delta V \quad (6)$$

[0210] Letting Cf0 be the value of capacitance Cf when the surface has a valley portion, and Cf1 be the value of capacitance Cf when the surface has a ridge portion (in this case, Cf0 < Cf1), the change amount difference ΔV due to the difference in surface shape is given by

20
$$\Delta V = (Cf1/(Cf1 + Cp) - Cf0/(Cf0 + Cp)) * \Delta V \quad (7)$$

[0211] The ridge and valley portions of the surface shape are detected by detecting the change amount difference ΔV due to the difference in surface shape by the detection circuit 120 and determining it.

25 [0212] As described above, the signal generation circuit changes the potential of the upper electrode 105 of the capacitance Cf in accordance with the detection timing to increase the voltage change corresponding to the change in capacitance Cf, thereby increasing the detection sensitivity.

[0213] Fig. 48 shows a case wherein the magnitude of the change amount difference ΔV due to the difference in surface shape is compared with that of the prior art.

30 [0214] Referring to Fig. 48, the abscissa represents the ratio of Cp to Cf0. As is apparent from Fig. 48, the change amount difference ΔV due to the difference in surface shape is larger in the device of the present invention. Hence, as compared to the conventional device, the signal change difference reflecting the ridge and valley portions of the surface shape can be made larger. As is apparent from Fig. 48, when the parasitic capacitance Cp is small, the change amount difference ΔV due to the difference in surface shape becomes large.

35 [0215] In the 27th embodiment shown in Fig. 46, the potential at the node N1 is set by the switch SW10. This is merely an example, and the potential can be set by another setting means. For example, the potential can be set by the transistor Q1a shown in Fig. 4.

[0216] In the signal generation circuit of the 27th embodiment, since a signal reflecting the three-dimensional pattern of the surface shape of an object to be measured is generated using capacitive coupling by the capacitance Cf, the signal change difference reflecting the three-dimensional pattern of the surface shape can be made larger than that of the prior art. In addition, since the capacitance Cs provided in the conventional device can be omitted, the parasitic capacitance Cp need not be estimated in designing, and cumbersome design of an appropriate capacitance Cs based on the estimated parasitic capacitance Cp is unnecessary. As a result, in this device, the fingerprint pattern detection accuracy can be prevented from lowering due to the manufacturing variation or power supply noise in the detection circuit 120, and a detection disable state can be prevented.

(28th Embodiment)

50 [0217] Fig. 49 shows a small capacitance change detection device according to the 28th embodiment of the present invention. Fig. 49 shows a section of one sensor element (detection element 10 shown in Fig. 2) in a sensor array two-dimensionally arrayed on a semiconductor substrate and the arrangement of a signal generation circuit 20 shown in Fig. 2.

[0218] The same reference numerals as in the small capacitance change detection device shown in Fig. 46 denote the same parts in Fig. 49, and a detailed description thereof will be omitted.

55 [0219] In the small capacitance change detection device shown in Fig. 46, a voltage Vs of an upper electrode 105 different from a lower electrode 104 connected to a node N1 of a capacitance Cf is controlled by a control means 130. In the small capacitance change detection device shown in Fig. 49, the potential of the upper electrode 105 is fixed (in this embodiment, ground potential GND).

[0220] The operation of the small capacitance change detection device shown in Fig. 49 will be described with reference to the timing charts in Figs. 50A to 50C.

[0221] Before a measurement object such as a finger 3 comes into contact with the two-dimensionally arrayed sensor array (i.e., in the non-contact state shown in Fig. 50B), at time ① in Fig. 50A, the control means 130 sets a control signal P at high level to turn on a switch SW10 to precharge the node N1 shown in Fig. 49 with an external voltage Vp, thereby charging the capacitance Cf. After the node N1 is precharged, at time ② in Fig. 50A, the control means 130 sets the control signal P at low level to turn off the switch SW10.

[0222] As shown in Fig. 50B, when the object to be measured partially comes into contact with the sensor, the value of the capacitance Cf changes, and consequently, the potential at the node N1 is changed by redistributing charges.

[0223] Letting Cf0 be the initial value of capacitance Cf, Cf0 be the value of capacitance Cf when the surface of the object to be measured has a valley portion, and Cf1 be the value of capacitance Cf when the surface of the object to be measured has a ridge portion (in this case, Cf0 < Cf1), the change amount difference ΔV due to the difference in surface shape is given by

$$\Delta V = ((Cf1 - Cf0) / (Cf1 + Cp) - (Cf0 - Cf1) / (Cf0 + Cp)) * Vp \quad (8)$$

[0224] The three-dimensional pattern of the surface shape of the object to be measured is detected by detecting the change amount difference ΔV due to the difference in surface shape by a detection circuit 120 and determining it.

[0225] In the signal generation circuit of the present invention, the capacitance Cf is precharged, and then, the object to be measured is brought into contact with the capacitance Cf to increase the voltage change corresponding to the change in capacitance Cf, thereby increasing the detection sensitivity.

[0226] Fig. 51 shows a case wherein the magnitude of the change amount difference ΔV due to the difference in surface shape is compared with that of the prior art.

[0227] Referring to Fig. 51, the abscissa represents the ratio of Cp to Cf0. As is apparent from Fig. 51, the change amount difference ΔV due to the difference in surface shape is larger in the device of the present invention. Hence, as compared to the conventional device, the signal change difference reflecting the three-dimensional pattern of the surface shape can be made larger. As is apparent from Fig. 51, when the parasitic capacitance Cp is small, the change amount difference ΔV due to the difference in surface shape becomes large.

[0228] In the 28th embodiment shown in Fig. 49, the potential at the node N1 is set by the switch SW10. This is merely an example, and the potential can be set by another setting means. For example, the potential can be set by the transistor Q1a shown in Fig. 4.

[0229] In the signal generation circuit of the 28th embodiment, since a signal reflecting the ridge and valley portions of the surface shape of an object to be measured is generated directly using the change in value of capacitance Cf when the object to be measured is in contact, the signal change difference reflecting the three-dimensional pattern of the surface shape can be made larger than that of the prior art. In addition, since the capacitance Cs provided in the conventional device can be omitted, the parasitic capacitance Cp need not be estimated in designing, and cumbersome design of an appropriate capacitance Cs based on the estimated parasitic capacitance Cp is unnecessary. As a result, in this device, the fingerprint pattern detection accuracy can be prevented from lowering due to the manufacturing variation or power supply noise in the detection circuit 120, and a detection disable state can be prevented. Furthermore, since signal generation can be started in synchronism with contact of the object to be measured, the signal generation timing signal need not be used.

(29th Embodiment)

[0230] Figs. 52A and 52B show a small capacitance change detection device according to the 29th embodiment of the present invention. Figs. 52A and 52B show arrangements of a sense unit 1 of this device. The same reference numerals as in Fig. 4 denote the same parts in Figs. 52A and 52B, and a detailed description thereof will be omitted.

[0231] In the sense unit 1 shown in Fig. 4, a detection element 10 formed from an electrostatic capacitance Cf between a sensor electrode 16 and the skin surface of a finger 3 is used. Instead, the sense unit 1 can also be constructed using a detection element 18 formed from a variable resistive element VR with elastic characteristics.

[0232] In this case, as shown in Fig. 52A, a first signal generation circuit 22, detection element 18, signal amplification circuit 30, and output circuit 40 are connected in series in the order named to construct the sense unit 1. The signal generation circuit 22 is formed from a capacitance Cs shown in Fig. 6. The signal amplification circuit 30 corresponds to the charge transfer signal amplification circuit 30 shown in Fig. 4.

[0233] The resistance value of the variable resistive element VR changes in accordance with deformation when an object such as the finger 3 to be recognized is in contact. The speed of removing charges stored by precharge by the capacitance Cs changes in accordance with the change in resistance value of the variable resistive element VR. When this change is detected as a voltage signal, the ridge and valley portions of the skin surface of a finger can be detected.

The remaining operations are basically the same as those of the sense unit 1 shown in Fig. 4.

[0234] As shown in Fig. 52B, a first signal generation circuit 23 constructed by a voltage source 24 and switch SW8 may be used in place of the signal generation circuit 22. The switch SW8 is connected between the variable resistive element VR and voltage source 24.

5 [0235] A voltage V of the voltage source 24 is set to have an arbitrary positive or negative value such that a current flows from the signal amplification circuit 30 to the signal generation circuit 23.

[0236] The ridge and valley portions of the skin surface of a finger can also be detected using the capacitance Cf instead of the detection element 18 shown in Figs. 52A and 52B. In this case, the first signal generation circuit, detection element (capacitance Cf) 10, signal amplification circuit 30, and output circuit 40 are connected in series in the order named.

10 [0237] Figs. 53A to 53C show other arrangements of the sense unit 1 shown in Figs. 52A and 52B. As shown in Fig. 53A, as a detection element 19, a switch element SW formed using the micromachine technology may be used. In this case, the signal generation circuit 23, detection element 19, signal amplification circuit 30, and output circuit 40 are connected in series in the order named to construct the sense unit 1.

15 [0238] The switch element SW opens/closes the circuit on the basis of contact of the object such as the finger 3 to be recognized. More specifically, when the switch element SW is depressed by a ridge portion of the skin surface of a finger, the signal generation circuit 23 and signal amplification circuit 30 are connected, and charges stored by precharge are removed by the voltage source 24. With this operation, the potential on the input side of the output circuit 40 lowers.

20 [0239] Conversely, when the switch element SW is depressed by a valley portion of the skin surface of a finger, the first signal generation circuit 23 and signal amplification circuit 30 are kept disconnected, and the potential on the input side of the output circuit 40 does not lower.

[0240] On the basis of this potential drop, the ridge and valley portions of the skin surface of a finger can be detected. The remaining operations are basically the same as those of the sense unit 1 shown in Fig. 4.

25 [0241] As shown in Fig. 53B or 53C, a signal generation circuit 20 including a current source 21a or signal generation circuit 22 including a capacitance Cs may be used.

[0242] The detection element 18 or 19 shown in Figs. 52A and 52B or 53A to 53C can be applied to any one of the sense units 1 shown in Figs. 8 and 10 to 13 together with a corresponding one of the signal generation circuits 20, 22, and 23. In the sense unit 1 shown in Fig. 13, however, the signal generation circuit 20, 22, or 23 need be set such that a current flows from the signal generation circuit 20, 22, or 23 to the signal amplification circuit 30.

30 [0243] As has been described above, according to the present invention, a small capacitance change detection device comprises a capacitance detection element, a signal generation circuit connected to the capacitance detection element to control predetermined charges, a signal amplification circuit connected to the connection portion between the signal generation circuit and capacitance detection element, and an output circuit. The signal amplification circuit has a transistor, a first voltage source connected to the control terminal of the transistor, a second voltage source, and a third voltage source. One of the second and third voltage sources is connected to the other output side of the transistor via a first switch. When the second voltage source is connected to the transistor, the voltage to be applied from the second voltage source to the other output side of the transistor is set to have a value equal to or larger than a value obtained by subtracting the threshold voltage of the transistor from the voltage of the first voltage source. When the third voltage source is connected to the transistor, the voltage to be applied from the third voltage source to the other output side of the transistor is set to have a value equal to or smaller than a value obtained by subtracting the threshold voltage of the transistor from the voltage of the first voltage source. The output circuit connected to the connection point between the other output side of the transistor and a first switch receives, after the voltage of the second or third voltage source is applied to the connection point in the ON state of the first switch, the voltage at the connection point on the basis of the OFF state of the first switch and charge control by the signal generation circuit after the first switch is turned off. With this arrangement, a small capacitance change detected by the capacitance detection element can be accurately extracted. Hence, the design margin of the output circuit can be increased.

Claims

50 1. A small capacitance change detection device characterized by comprising:

a capacitance detection element (10) for detecting a small capacitance change;
 a signal generation circuit (20) having an output side connected to said capacitance detection element to control predetermined charges;
 55 a signal amplification circuit (30) having an input side connected to a connection point between the output side of said signal generation circuit and said capacitance detection element; and
 an output circuit (40) connected to an output side of said signal amplification circuit,
 said signal amplification circuit comprising

a first transistor (Q2a) having one output terminal connected to the connection portion between the output side of said signal generation circuit and said capacitance detection element,
 5 a first voltage source (Vg) connected to a control terminal of said first transistor,
 a second voltage source (VDD), and
 a third voltage source (GND),
 wherein one of said second and third voltage sources is connected to the other output terminal of said first transistor via a first switch (Q1a),
 10 a voltage to be applied from said second voltage source to the other output terminal of said first transistor is set to have a value not less than a value obtained by subtracting a threshold voltage of said first transistor from a voltage of said first voltage source that is applied to the control terminal of said first transistor while a voltage to be applied from said third voltage source to the other output terminal of said first transistor is set to have a value not more than a value obtained by subtracting the threshold voltage of said first transistor from the voltage of said first voltage source that is applied to the control terminal of said first transistor, and
 15 said output circuit is connected to a connection point between the other output terminal of said first transistor and said first switch and, after a voltage of one of said second and third voltage sources is applied to the connection point in an ON state of said first switch, receives the voltage at the connection point on the basis of an OFF state of said first switch and charge control by said signal generation circuit after said first switch is turned off.

20 2. A device according to claim 1, wherein

25 said signal generation circuit and said signal amplification circuit are arranged near said capacitance detection element.

30 3. A device according to claim 2, wherein

35 said output circuit is arranged near said signal amplification circuit.

40 4. A device according to claim 1, wherein

45 said signal generation circuit is shared by a plurality of capacitance detection elements close to each other.

50 5. A device according to claim 1, wherein

55 said signal amplification circuit is shared by a plurality of capacitance detection elements close to each other.

60 6. A device according to claim 1, wherein

65 said output circuit is shared by a plurality of capacitance detection elements close to each other.

70 7. A device according to claim 1, wherein

75 said signal generation circuit, said signal amplification circuit, and said output circuit are arranged in units of capacitance detection elements.

80 8. A device according to claim 1, wherein

85 said device further comprises a reference signal generation circuit (50) connected to the input side of said signal amplification circuit to generate a reference signal, and

90 said signal amplification circuit comprises a circuit (31) having a gain changing means for changing a gain on the basis of comparison between a level of an output signal from said signal generation circuit and that of the reference signal.

95 9. A device according to claim 8, wherein

100 said gain changing means decreases the gain when the level of the output signal from said signal generation circuit is lower than that of the reference signal, and increases the gain when the level of the output signal from said signal generation circuit is higher than that of the reference signal.

10. A device according to claim 8, wherein

5 said gain changing means increases the gain when the level of the output signal from said signal generation circuit is lower than that of the reference signal, and decreases the gain when the level of the output signal from said signal generation circuit is higher than that of the reference signal.

11. A device according to claim 8, wherein

10 the reference signal has the same level as that of the signal output from said signal generation circuit in correspondence with a predetermined quantity of electricity of said capacitance detection element.

12. A device according to claim 8, wherein

15 said reference signal generation circuit comprises a reference element (51) having a predetermined quantity of electricity, and a reference signal generation section (52) for generating the reference signal corresponding to the predetermined quantity of electricity of said reference element, said reference signal generation section having the same arrangement as that of said signal generation circuit.

20 13. A device according to claim 12, wherein

25 said signal amplification circuit comprises a second transistor (Q2b) having one output terminal connected to a connection point between said reference element and said reference signal generation section, the other output terminal connected to said second voltage source via a second switch (Q1b), and a control terminal connected to the connection point between the other output terminal of said first transistor and said first switch, and having the same characteristics as those of said first transistor, and said second voltage source is connected to the control terminal of said first transistor via said second switch as the first voltage source.

30 14. A device according to claim 13, wherein

35 said output circuit comprises a differential output circuit (40a) having input sides connected to the other output terminal of said first transistor and the other output terminal of said second transistor, respectively.

35 15. A device according to claim 13, wherein

40 said signal amplification circuit comprises a third switch (Q9) connected between the other output terminal of said first transistor and that of said second transistor to short-circuit the other output terminal of said first transistor to that of said second transistor in an inoperative state of said signal generation circuit and said reference signal generation section and disconnect the other output terminal of said first transistor from that of said second transistor in an operative state of said signal generation circuit and said reference signal generation section.

45 16. A device according to claim 8, wherein

45 said reference signal generation circuit is arranged near a corresponding signal amplification circuit.

50 17. A device according to claim 8, wherein said reference signal generation circuit is shared by a plurality of signal amplification circuits close to each other.

50 18. A device according to claim 8, wherein

55 said reference signal generation circuit is arranged in units of signal amplification circuits.

55 19. A device according to claim 8, wherein

55 said device further comprises a plurality of lower electrodes (104) formed on a substrate (101) to be insulated and isolated from each other,

an upper electrode (105) formed to oppose said lower electrodes,
 a support member (103) formed on said substrate in units of lower electrodes to support said upper electrode, and
 5 a reference electrode (104a) formed between each of said lower electrodes on said substrate and said support member to be separated from said lower electrode and said support member,
 said upper electrode can be deformed in a direction of the lower electrodes using said support member as a fulcrum, and
 10 said capacitance detection element detects a capacitance between said upper electrode and said lower electrode while said reference signal generation circuit detects a capacitance between said upper electrode and said reference electrode to output the reference signal.

20. A device according to claim 19, wherein

surfaces of said lower electrode and said reference electrode opposing said upper electrode have the same
 15 area.

21. A device according to claim 19, wherein

said reference electrode is formed to surround said lower electrode.

22. A device according to claim 19, wherein

said plurality of lower electrodes are formed in a matrix.

25 23. A device according to claim 19, wherein

said support member has a matrix shape, and said lower electrode is formed at a central portion of each square.

30 24. A device according to claim 1, wherein

said signal generation circuit comprises
 a fourth switch (Q3a) connected to the connection portion, and
 35 a current source (21a) connected to said fourth switch to remove predetermined charges at the connection portion on the basis of an ON state of said fourth switch.

25. A device according to claim 1, wherein

said signal generation circuit comprises
 40 a fifth switch (SW1) connected to the connection portion, and
 a capacitive element having a capacitance value C_s , said capacitive element normally removing stored charges and, upon being connected to the connection portion through said fifth switch, charging the connection portion.

45 26. A device according to claim 1, wherein

said signal generation circuit comprises a capacitive element having a first terminal connected to the connection portion and a second terminal, said capacitive element having a capacitance value (C_s), and
 50 said signal generation circuit sets the second terminal of said capacitive element at a first potential while said capacitance detection element is charged and then changes the second terminal to a second potential to make said capacitance detection element to generate a voltage signal.

27. A device according to claim 26, wherein

55 letting C_p be a parasitic capacitance value generated in the first terminal of said capacitive element, and C_{fv} and C_{fr} be maximum and minimum capacitance values of said capacitance detection element, respectively, the capacitance value C_s of said capacitive element is set to be $\{(C_{fv} + C_p)(C_{fr} + C_p)\}^{1/2}$.

28. A device according to claim 26, wherein

the capacitance value (Cs) of said capacitive element is set to be not more than a maximum value of a capacitance value of said capacitance detection element.

5 29. A device according to claim 26, wherein

the capacitance value (Cs) of said capacitive element has a range from 10 fF to 250 fF.

10 30. A device according to claim 1, wherein

said output circuit comprises a voltage-time conversion circuit (141) for converting an input voltage signal into a time signal.

15 31. A device according to claim 1, wherein

said output circuit comprises
a first output circuit (140), and
a bias adjusting circuit (160) for adjusting a threshold voltage of said first output circuit.

20 32. A device according to claim 30, further comprising a threshold adjusting circuit (161) for adjusting a threshold voltage of said voltage-time conversion circuit.

25 33. A device according to claim 30, wherein

said voltage-time conversion circuit comprises
a variable current source (43) whose current amount changes in accordance with the input voltage,
a capacitive element having a capacitance value (CL) charged/discharged on the basis of a current of said variable current source, and
30 a threshold circuit (42) whose output voltage changes depending on whether the input voltage exceeds the threshold voltage.

34. A device according to claim 33, wherein

35 said threshold circuit comprises a Schmidt trigger circuit.

36. A device according to claim 31, wherein

40 said first output circuit has a variable threshold circuit (45), and
a threshold adjusting circuit (161) for adjusting a threshold voltage of said variable threshold circuit is used as said bias adjusting circuit.

36. A device according to claim 35, wherein

45 said variable threshold circuit comprises a Schmidt trigger circuit.

37. A device according to claim 35, wherein

50 said variable threshold circuit comprises an element (47, 47a) for determining the threshold voltage value, and
said threshold adjusting circuit adjusts a potential of at least one of nodes (N4, N6) of said element.

38. A device according to claim 32, wherein

55 said voltage-time conversion circuit comprises a variable threshold circuit (45), and
said threshold adjusting circuit adjusts a threshold voltage of said variable threshold circuit.

39. A device according to claim 38, wherein

said variable threshold circuit comprises a Schmidt trigger circuit.

40. A device according to claim 38, wherein

5 said variable threshold circuit comprises an element (47, 47a) for determining the threshold voltage value, and said threshold adjusting circuit adjusts a potential of at least one of nodes (N4, N6) of said element.

41. A device according to claim 37, wherein

10 said device further comprises, as elements for determining the threshold voltage value, a plurality of conductive elements (47, Q13, 47a, Q14) for dividing a voltage, applied to the node, by an ON resistance ratio, and said threshold adjusting circuit controls a value of the voltage to be applied to the node of said element and determines the threshold voltage value using the divided voltage divided by said plurality of conductive elements.

15 42. A device according to claim 37, further comprising at least one conductive element (49) added between the node and a power supply voltage of said variable threshold circuit.

43. A device according to claim 37, wherein

20 said device further comprises, as elements for determining the threshold voltage value, a plurality of conductive elements (47, 49, Q13) for dividing a voltage, applied to the node, by an ON resistance ratio, and said threshold adjusting circuit controls an ON resistance value of at least one of said conductive elements through the node and determines the threshold voltage value using the divided voltage divided by said plurality of conductive elements.

25 44. A device according to claim 37, wherein

30 the nodes for controlling the threshold voltage value from the outside of said variable threshold circuit are connected to connect a plurality of variable threshold circuits.

45. A device according to claim 44, further comprising a conductive element (48) connected between the nodes connected to connect said plurality of variable threshold circuits and a power supply voltage of said variable threshold circuits.

35 46. A device according to claim 40, wherein

40 said device further comprises, as elements for determining the threshold voltage value, a plurality of conductive elements (47, Q13, 47a, Q14) for dividing a voltage, applied to the node, by an ON resistance ratio, and said threshold adjusting circuit controls a value of the voltage to be applied to the node of said element and determines the threshold voltage value using the divided voltage divided by said plurality of conductive elements.

45 47. A device according to claim 40, further comprising at least one conductive element (49) added between the node and a power supply voltage of said variable threshold circuit.

48. A device according to claim 40, wherein

50 said device further comprises, as elements for determining the threshold voltage value, a plurality of conductive elements (47, 49, Q13) for dividing a voltage, applied to the node, by an ON resistance ratio, and said threshold adjusting circuit controls an ON resistance value of at least one of said conductive elements through the node and determines the threshold voltage value using the divided voltage divided by said plurality of conductive elements.

55 49. A device according to claim 40, wherein

the nodes for controlling the threshold voltage value from the outside of said variable threshold circuit are connected to connect a plurality of variable threshold circuits.

50. A device according to claim 49, further comprising a conductive element (48) connected between the nodes connected to connect said plurality of variable threshold circuits and a power supply voltage of said variable threshold circuits.

5 51. A device according to claim 1, wherein
said capacitance detection element detects a capacitance change corresponding to ridge and valley portions of a skin surface of a finger.

10 52. A small capacitance change detection device characterized by comprising:
a capacitance detection element (10) for detecting a small capacitance change;
a signal generation circuit (20) having an output side connected to said capacitance detection element to control predetermined charges;
15 an output circuit (120) having an input side connected to a connection point between the output side of said signal generation circuit and said capacitance detection element;
a plurality of lower electrodes (104) formed on a substrate (101) to be insulated and isolated from each other;
20 an upper electrode (105) formed to oppose said lower electrodes; and
a support member (103) formed on said substrate in units of lower electrodes to support said upper electrode,
said signal generation circuit comprising
setting means for setting a potential at the connection portion, and
control means (130) for controlling said upper electrode to a predetermined potential and operating said setting means to set a predetermined voltage at said lower electrode, then controlling said setting means in an inoperative state to disconnect an external voltage source from said lower electrode, and changing the potential of
25 said upper electrode to a potential different from the predetermined potential,
wherein said output circuit receives a voltage of said lower electrode based on a capacitance between said upper electrode and said lower electrode, which is generated from said capacitance detection element when
said setting means is set in the inoperative state and the potential of said upper electrode changes to a potential different from the predetermined potential.

30 53. A device according to claim 52, wherein
said setting means comprises a sixth switch (SW10) connected between said external voltage source (Vp) and the connection portion, and
35 said control means controls said upper electrode to a predetermined potential and turns on said sixth switch to apply a voltage of said external voltage source to said lower electrode, then turns off said sixth switch, and changes the potential of said upper electrode changes to a potential different from the predetermined potential.

40 54. A device according to claim 52, wherein
said control means individually controls potentials of a plurality of upper electrodes and lower electrodes.

45 55. A device according to claim 52, wherein
said capacitance detection element detects a capacitance change corresponding to ridge and valley portions of a skin surface of a finger.

50 56. A small capacitance change detection device characterized by comprising:
a capacitance detection element (10) for detecting a small capacitance change;
a signal generation circuit (20) having an output side connected to said capacitance detection element to control predetermined charges;
an output circuit (120) having an input side connected to a connection point between the output side of said signal generation circuit and said capacitance detection element;
55 a plurality of lower electrodes (104) formed on a substrate (101) to be insulated and isolated from each other;
an upper electrode (105) formed to oppose said lower electrodes; and
a support member (103) formed on said substrate in units of lower electrodes to support said upper electrode,
wherein said upper electrode can deform in a direction of lower electrode using said support member as a ful-

crum and is held at a predetermined potential,
said signal generation circuit comprises
setting means for setting a potential at the connection portion, and
control means (130) for operating said setting means to set a predetermined voltage at said lower electrode
5 and then controlling said setting means in an inoperative state to disconnect an external voltage source from
said lower electrode, and
said output circuit receives a voltage of said lower electrode based on a capacitance between said upper electrode and said lower electrode, which is generated when said capacitance detection element deforms after
said setting means is set in the inoperative state.

10 57. A device according to claim 56, wherein

said setting means comprises a sixth switch (SW10) connected between said external voltage source (Vp) and
the connection portion, and
15 said control means turns on said sixth switch to apply a voltage of said external voltage source to said lower electrode and then turns off said sixth switch.

58. A device according to claim 56, wherein

20 said control means individually controls potentials of said plurality of lower electrodes.

59. A device according to claim 56, wherein

25 said capacitance detection element detects a capacitance change corresponding to ridge and valley portions of a skin surface of a finger.

60. A small capacitance change detection device characterized by comprising:

30 a capacitance detection element (10) for detecting a small capacitance change;
a signal generation circuit (20) having an output side connected to one terminal of said capacitance detection element to control charges;
a signal amplification circuit (30) having an input side connected to the other terminal of said capacitance detection element; and
35 an output circuit (40) connected to an output side of said signal amplification circuit,
wherein said signal amplification circuit receives a voltage change at the other terminal of said capacitance detection element based on charge control by said signal generation circuit.

61. A device according to claim 60, wherein

40 said capacitance detection element detects a capacitance change corresponding to ridge and valley portions of a skin surface of a finger.

45

50

55

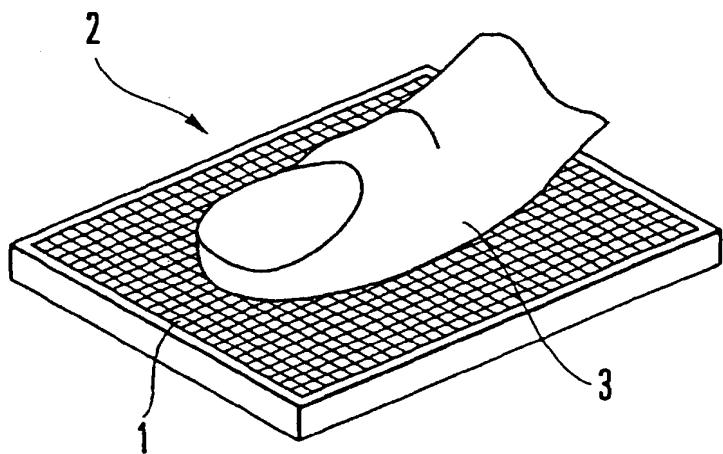


FIG. 1

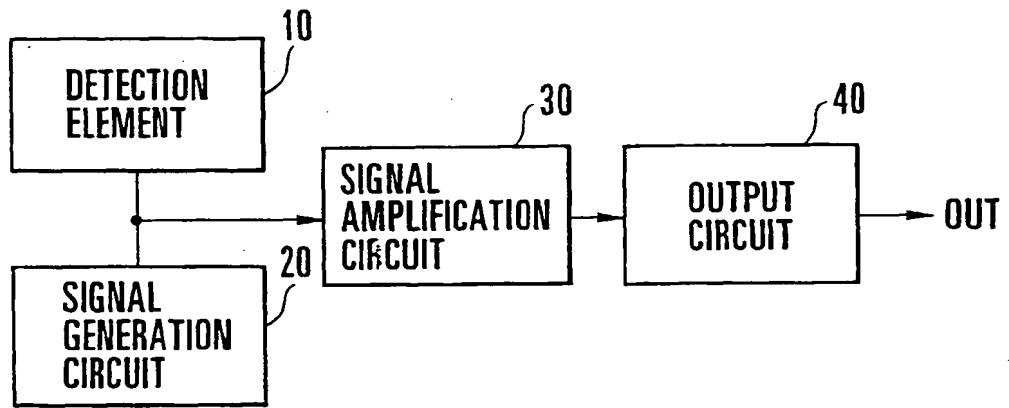


FIG. 2

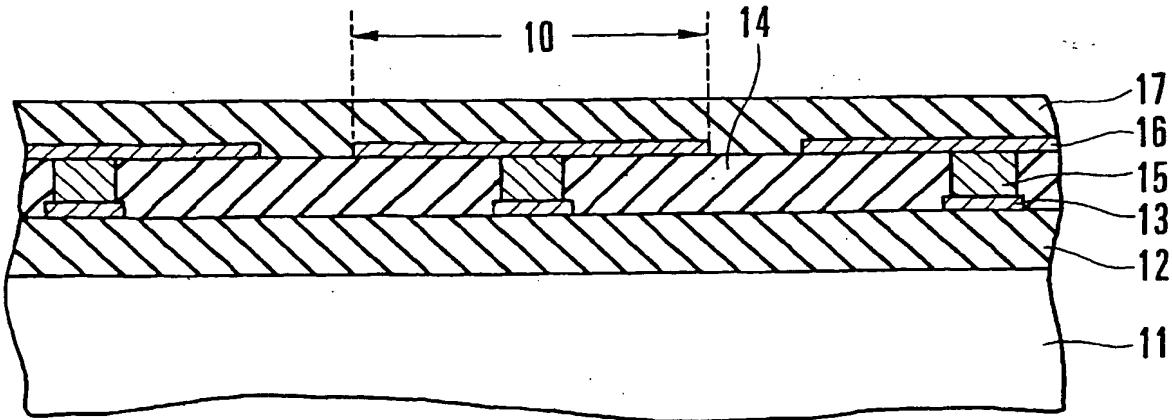


FIG. 3

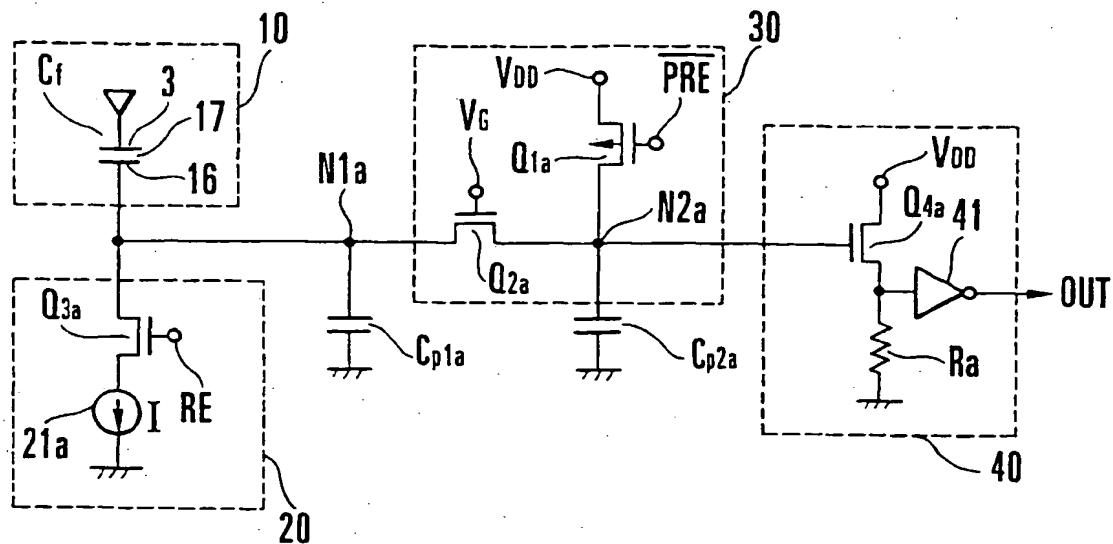


FIG. 4

FIG. 5A

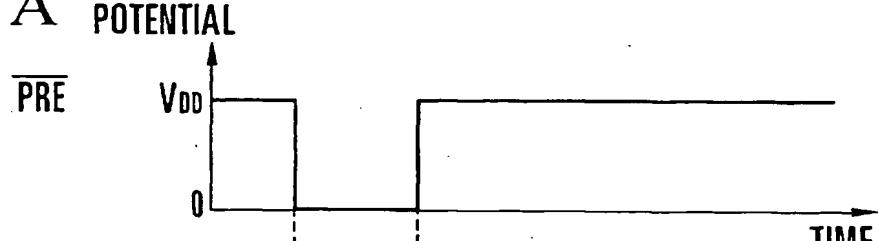


FIG. 5B

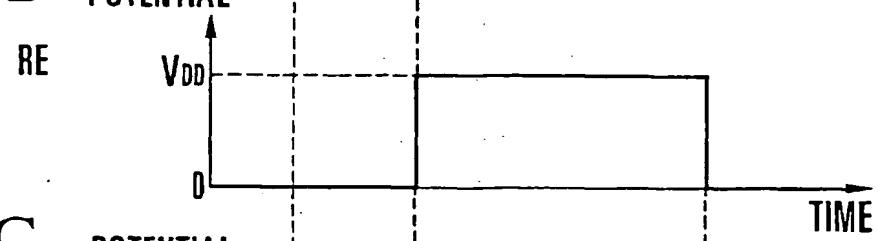
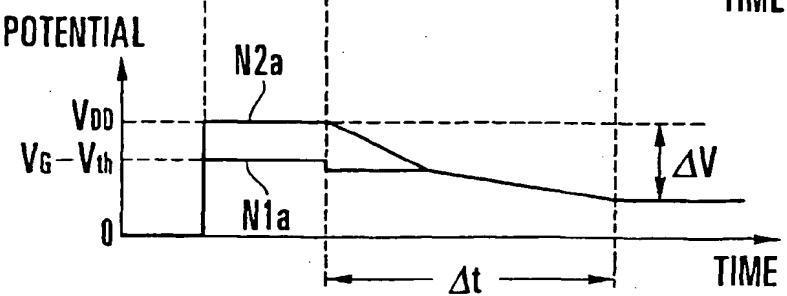


FIG. 5C

N1a, N2a



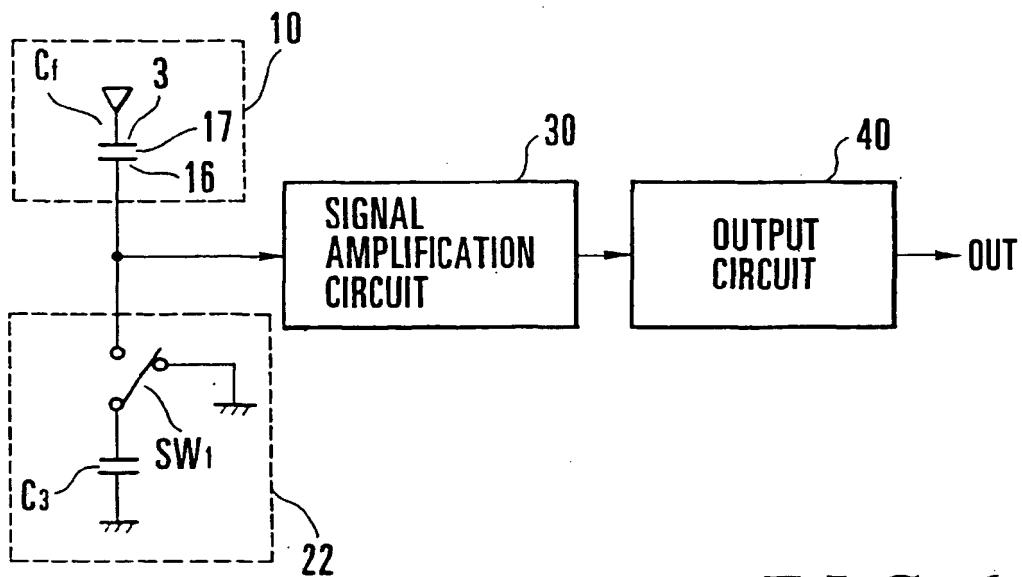


FIG. 6

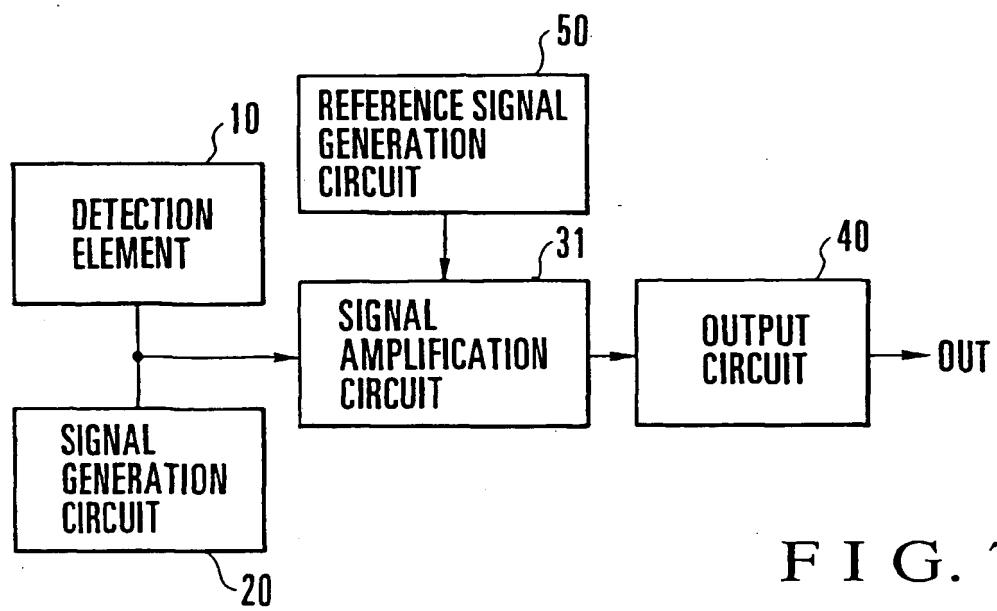


FIG. 7

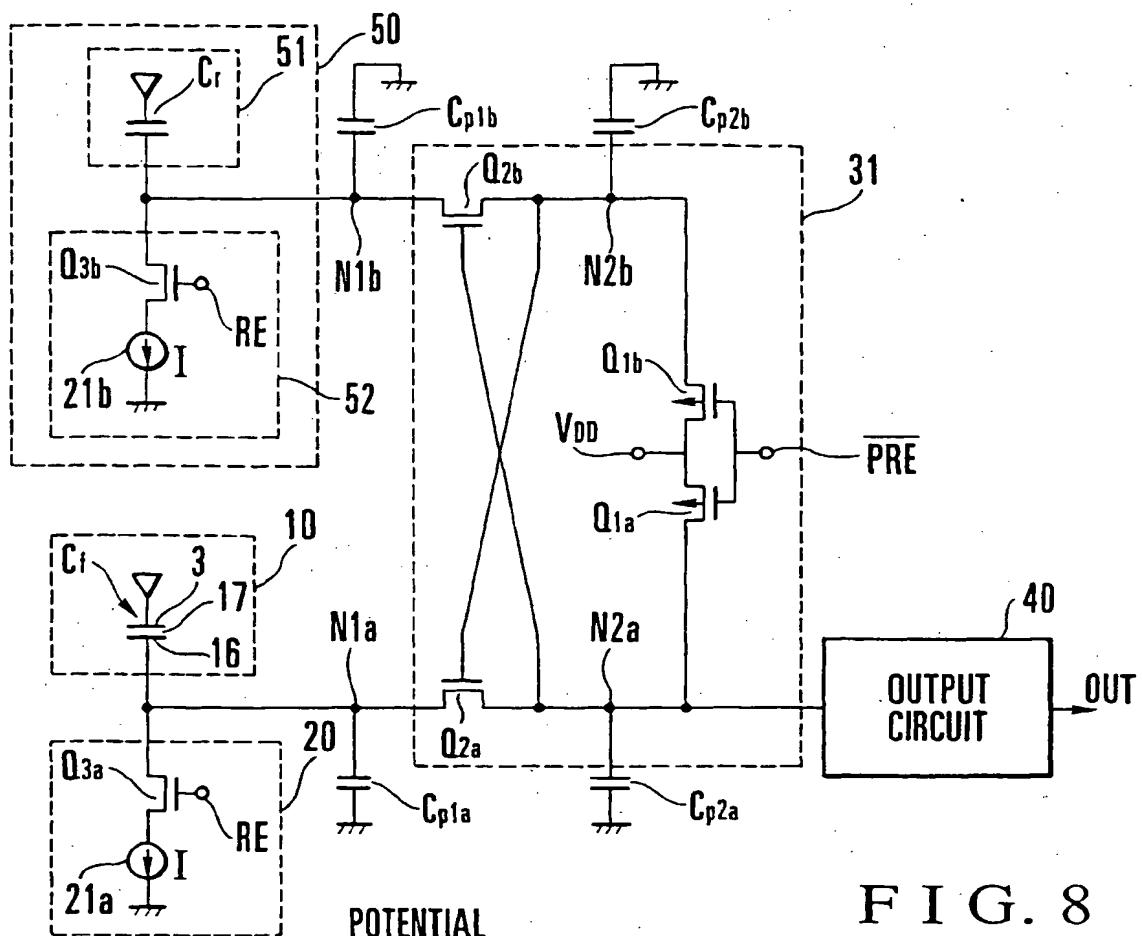


FIG. 8

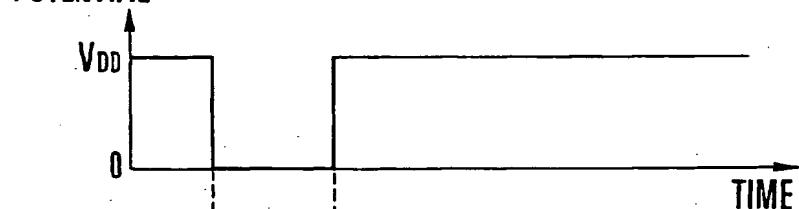
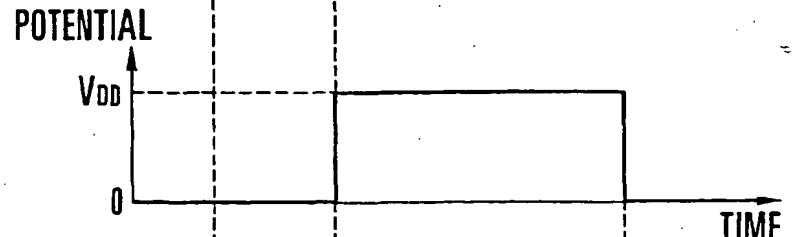
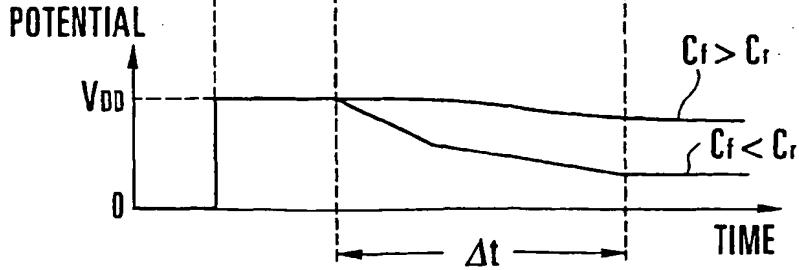
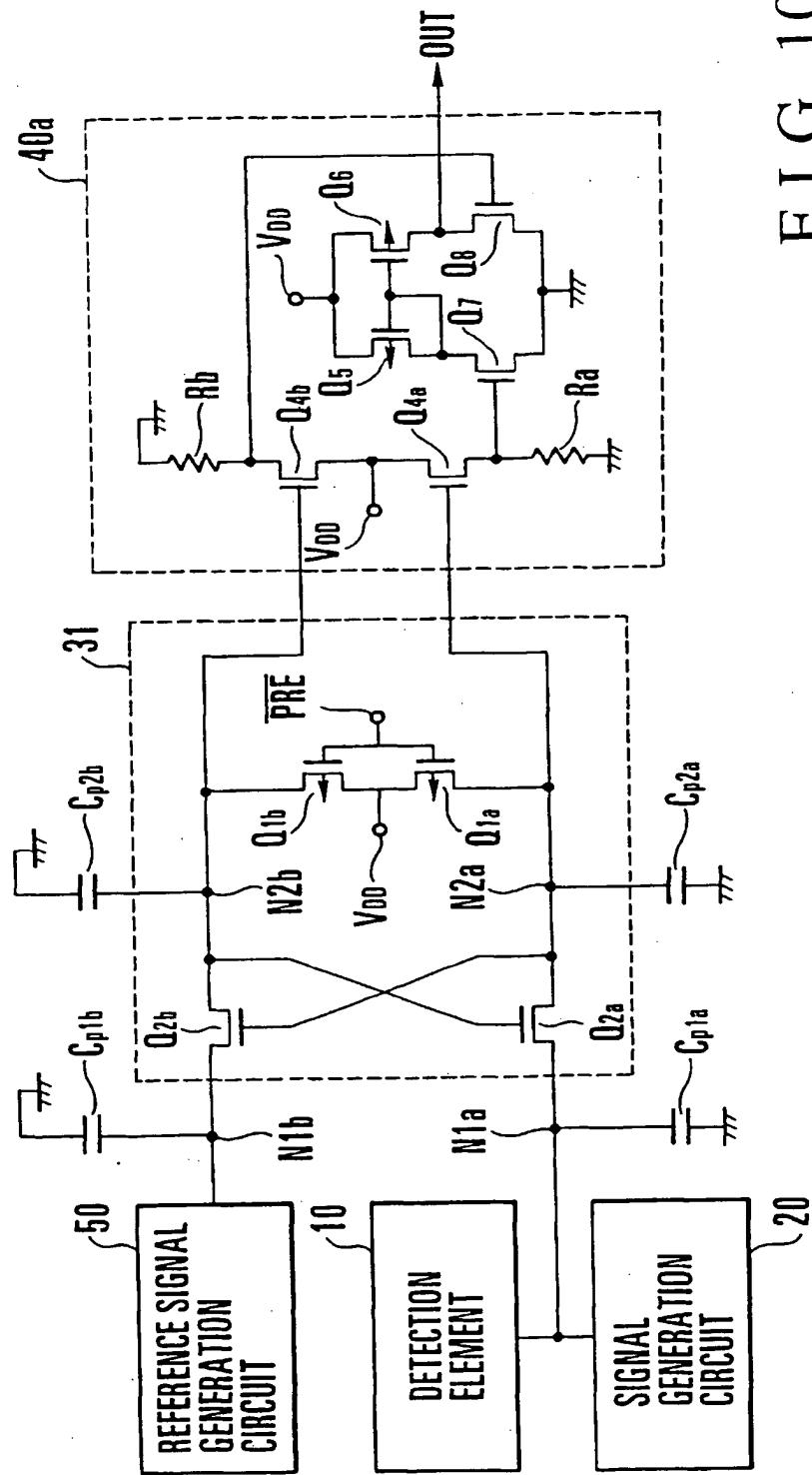
FIG. 9A
PREFIG. 9B
REFIG. 9C
N2a

FIG. 10



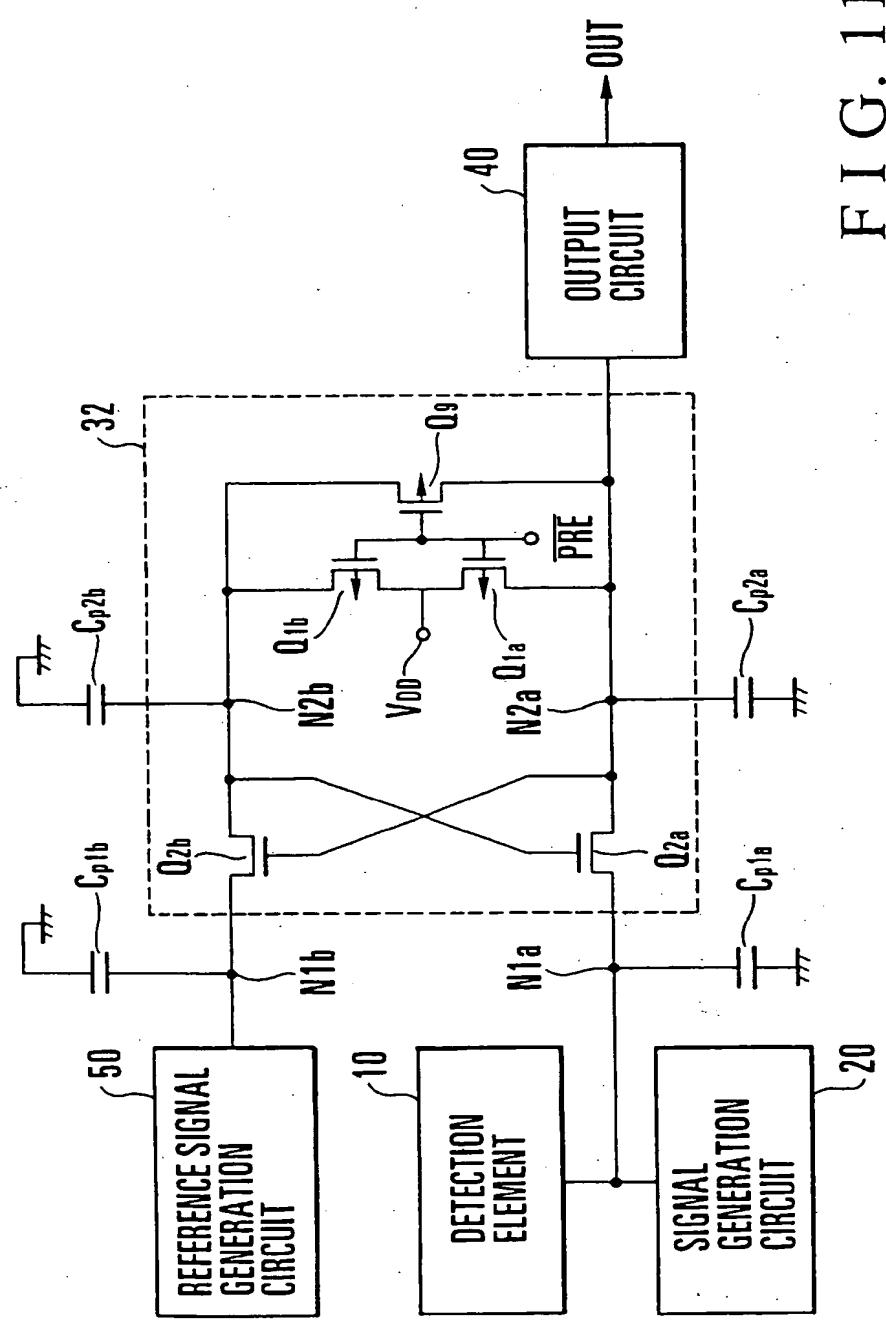


FIG. 11

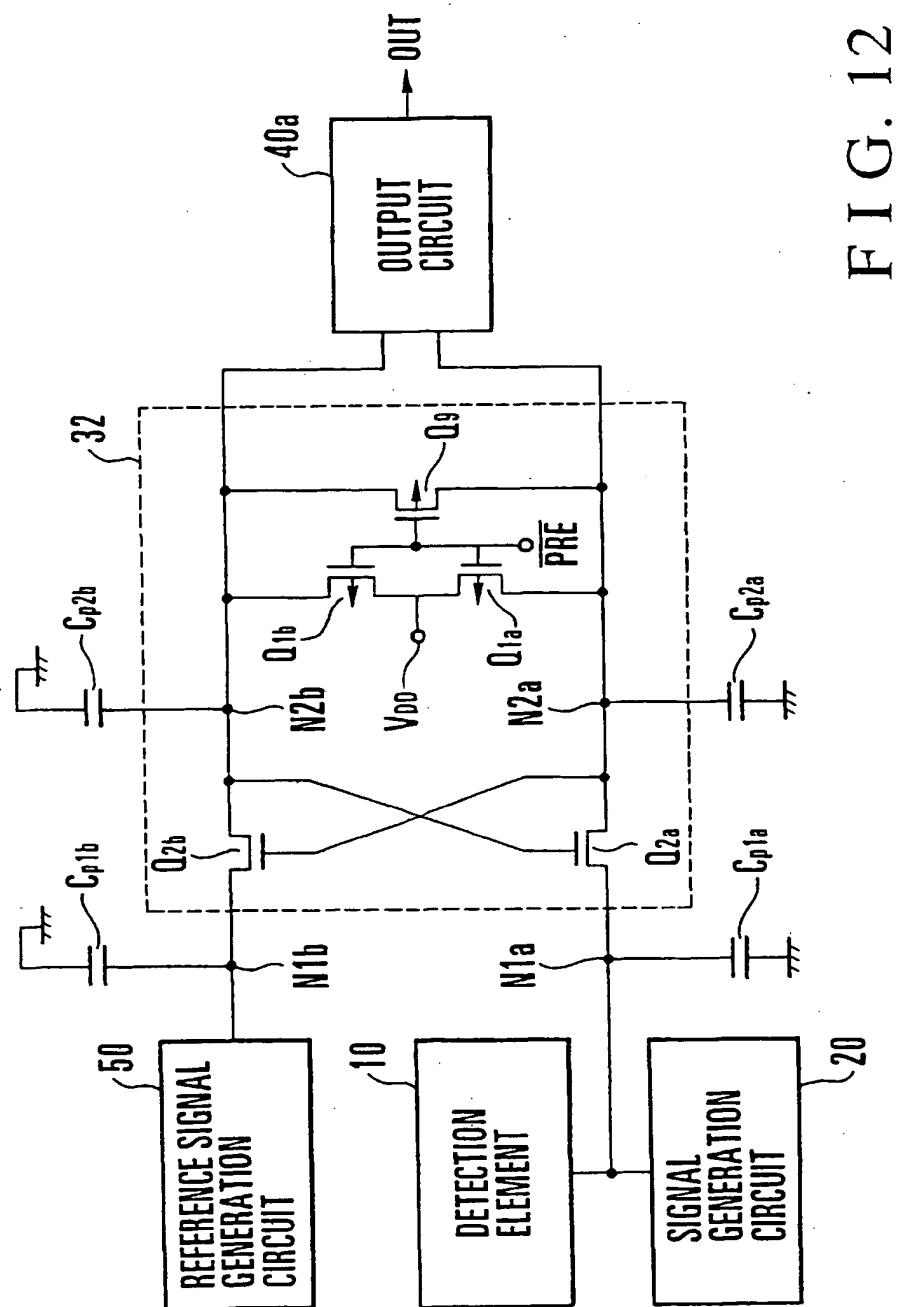


FIG. 12

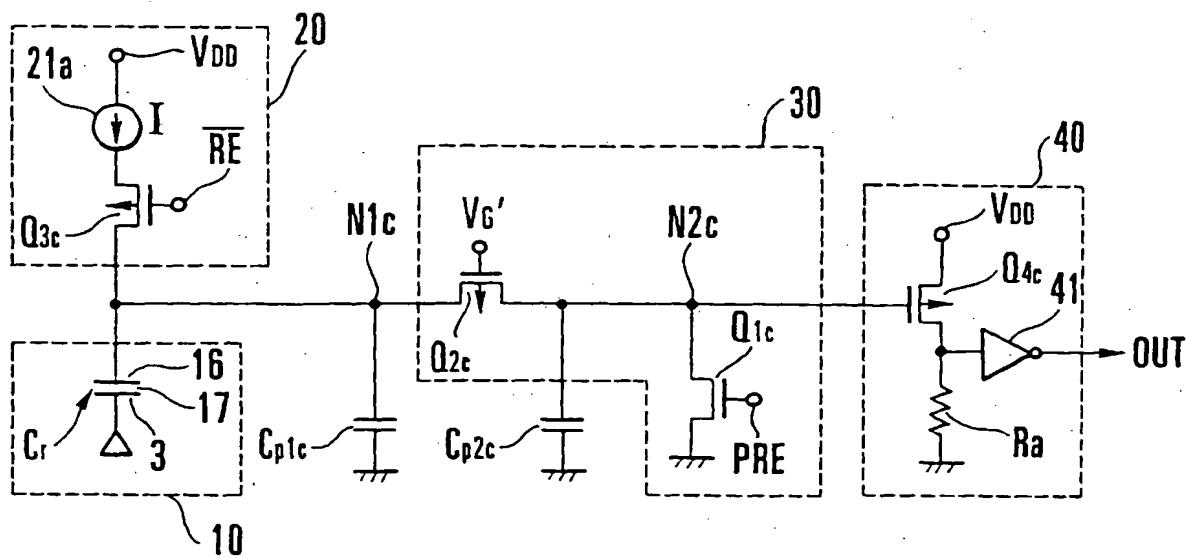


FIG. 13

FIG. 14A POTENTIAL

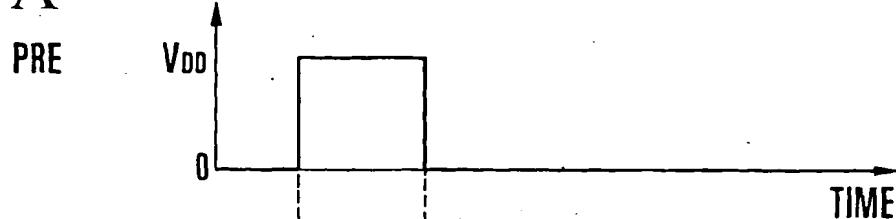


FIG. 14B POTENTIAL

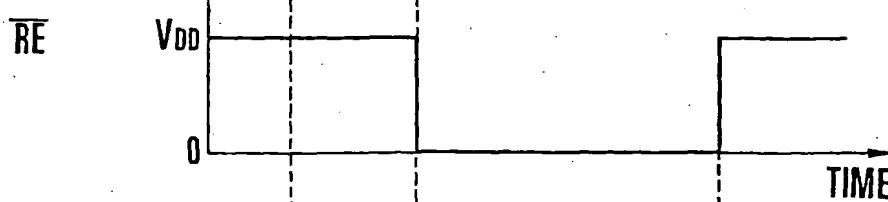
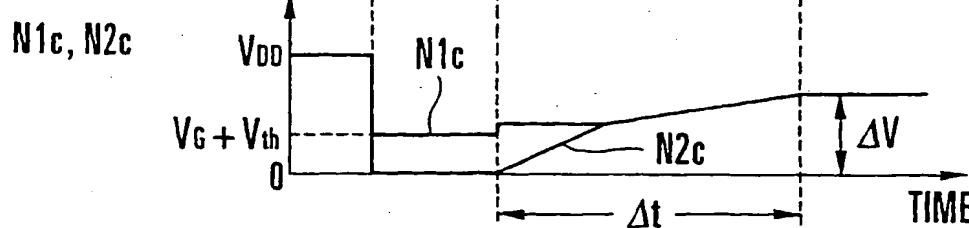


FIG. 14C POTENTIAL



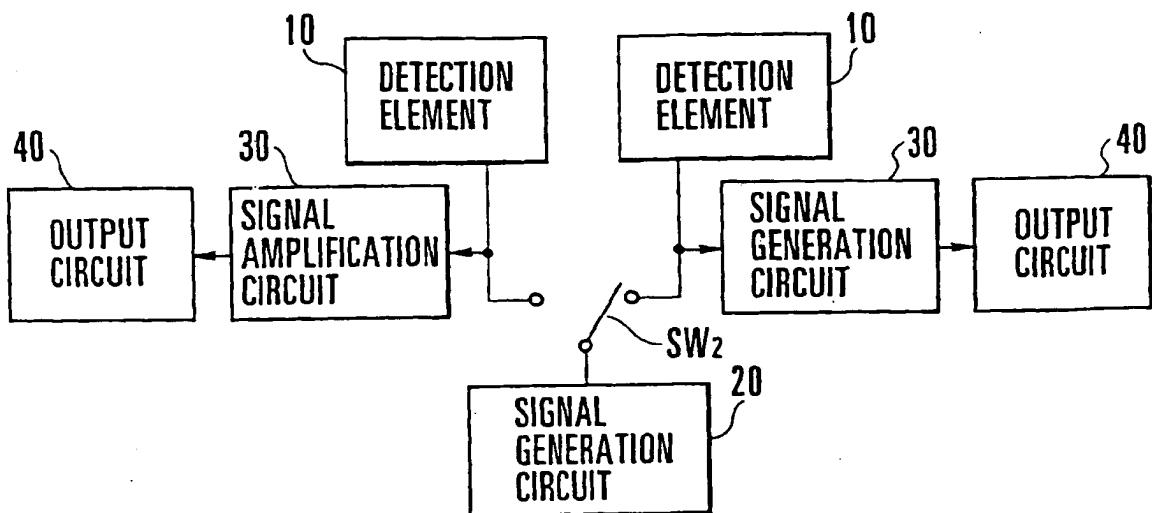


FIG. 15A

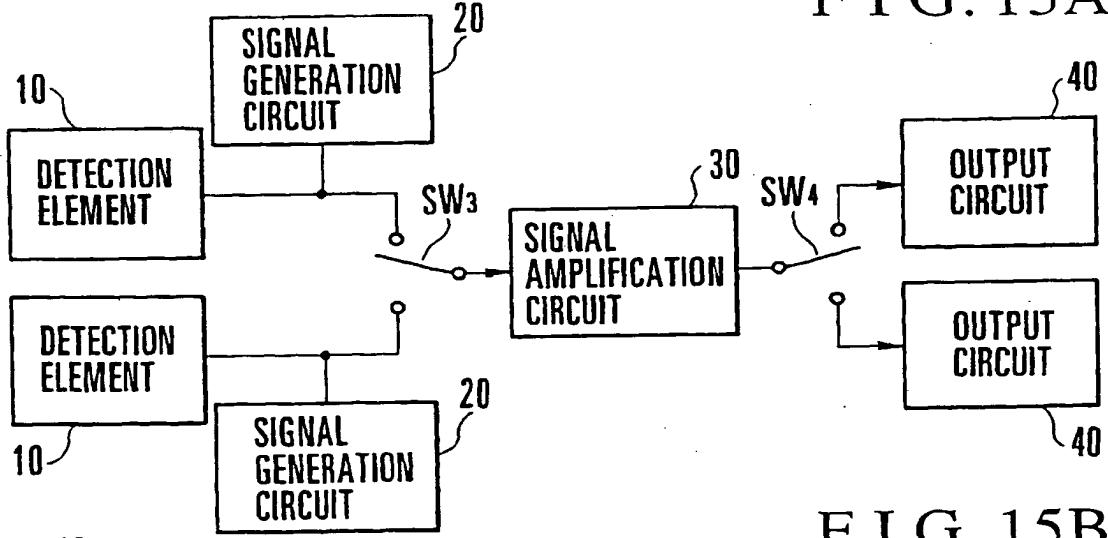


FIG. 15B

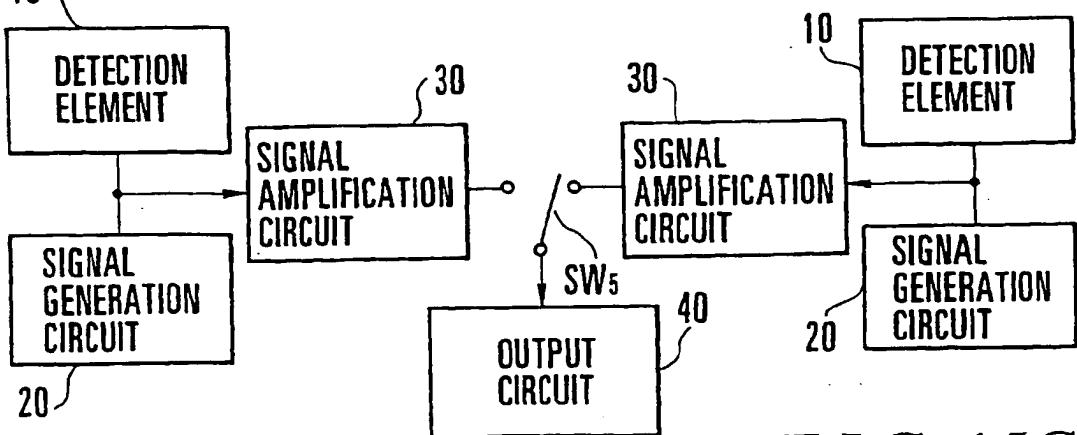


FIG. 15C

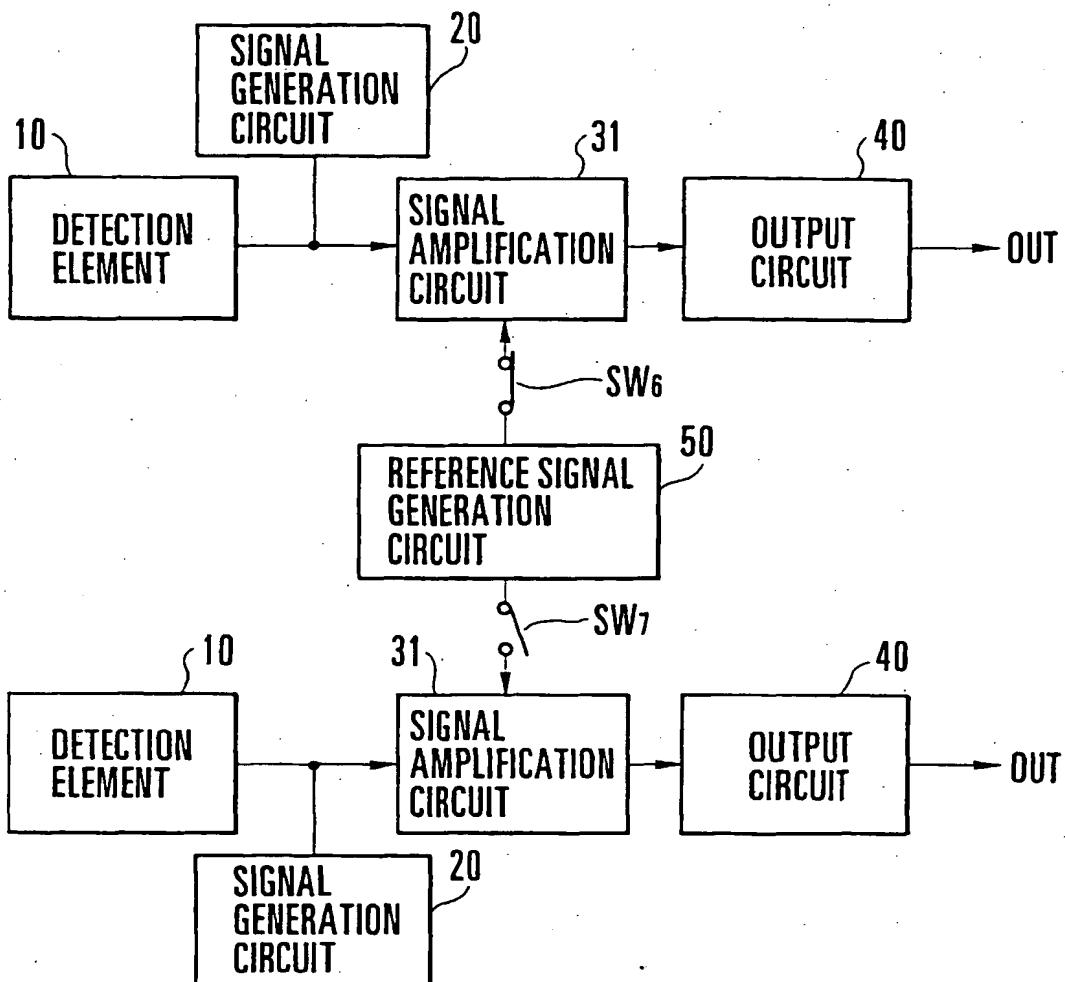


FIG. 16

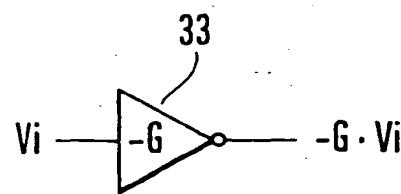


FIG. 17A

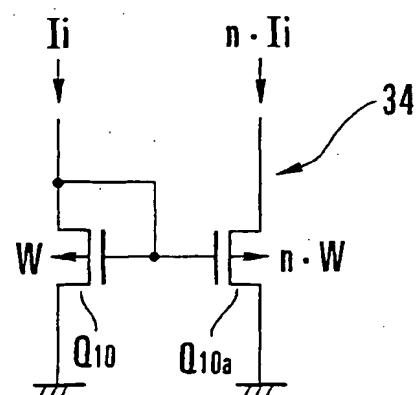


FIG. 17B

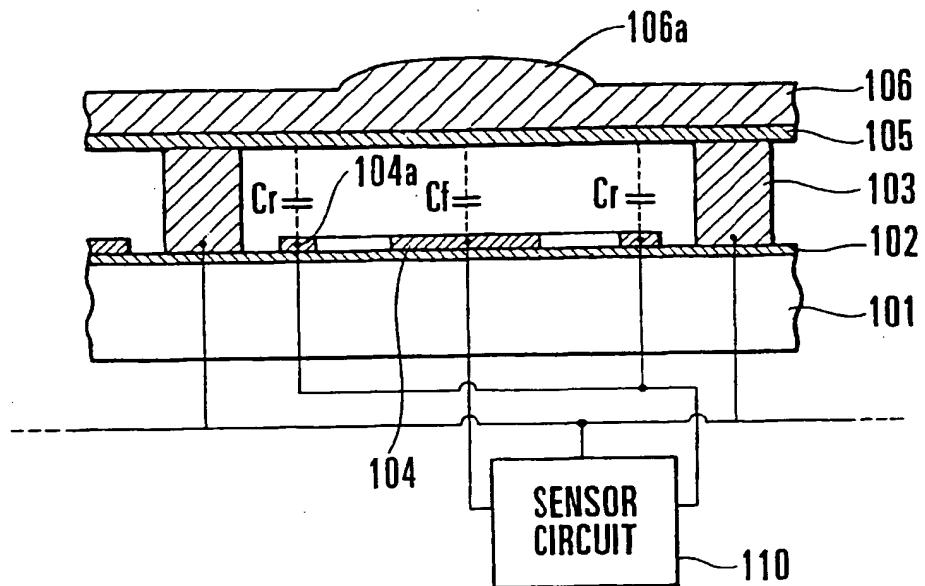


FIG. 18A

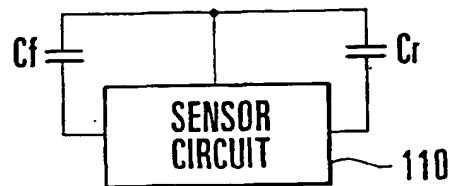


FIG. 18B

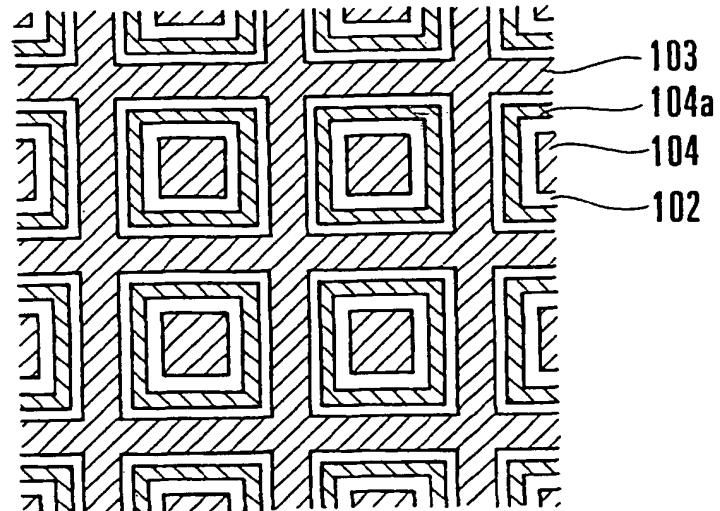


FIG. 19

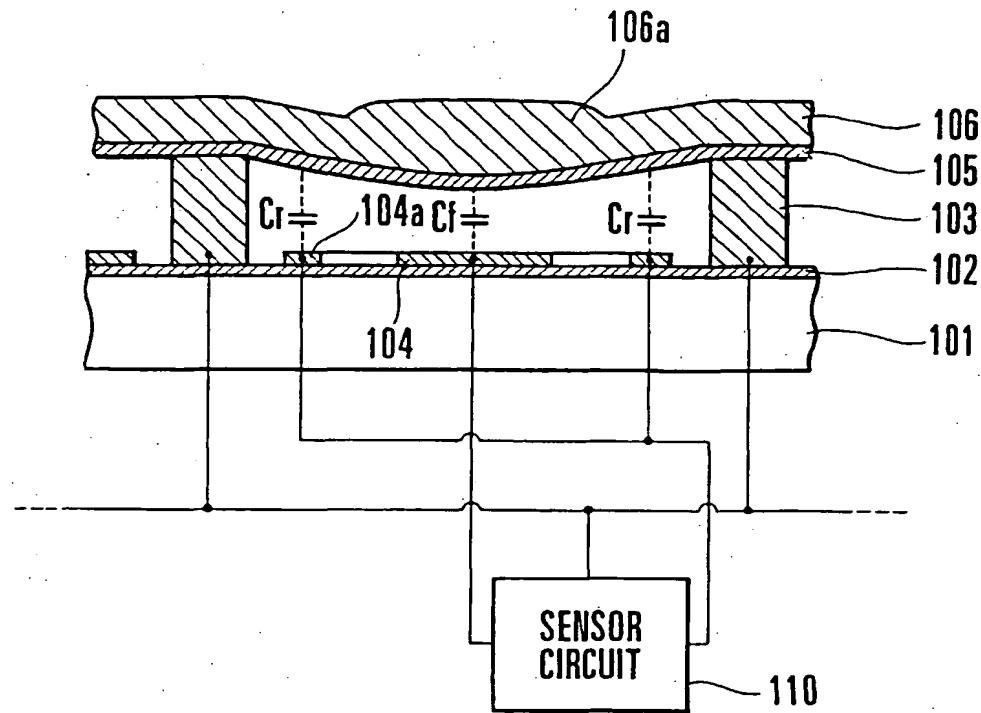


FIG. 20

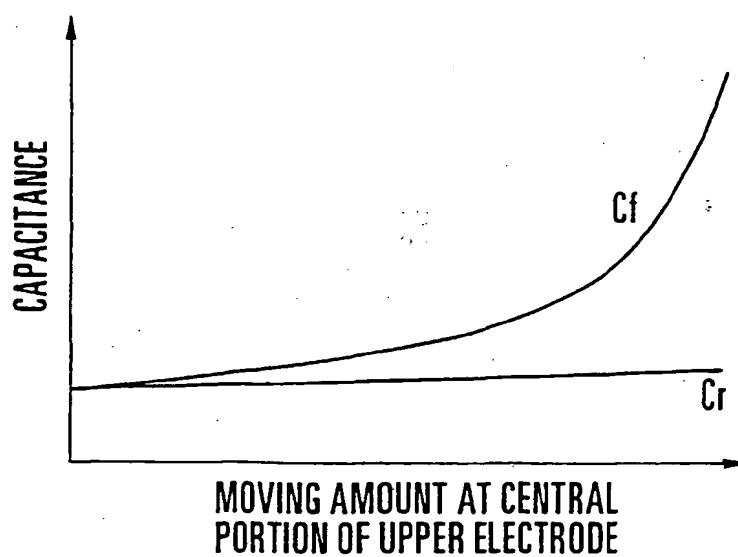


FIG. 21

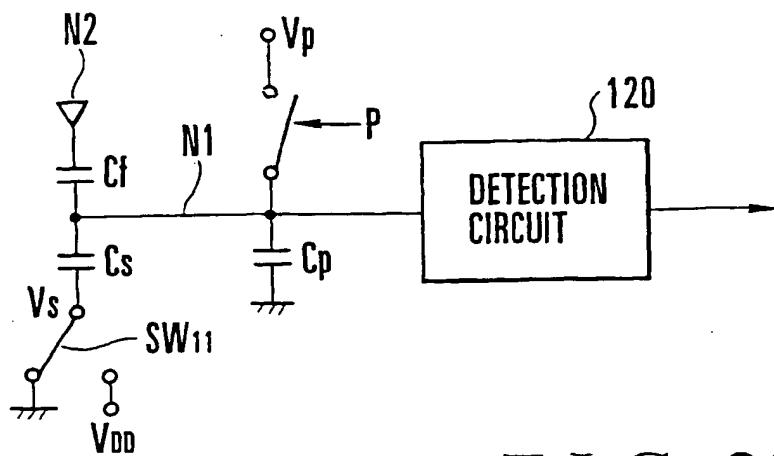
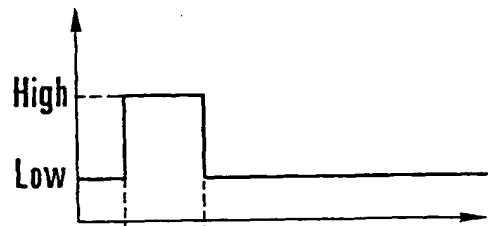
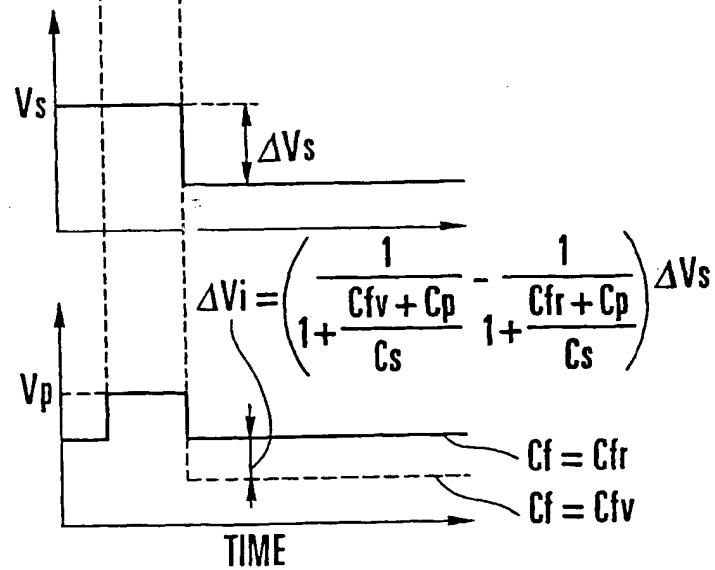


FIG. 22

FIG. 23A
POTENTIAL PFIG. 23B
POTENTIAL VsFIG. 23C
POTENTIAL AT N1

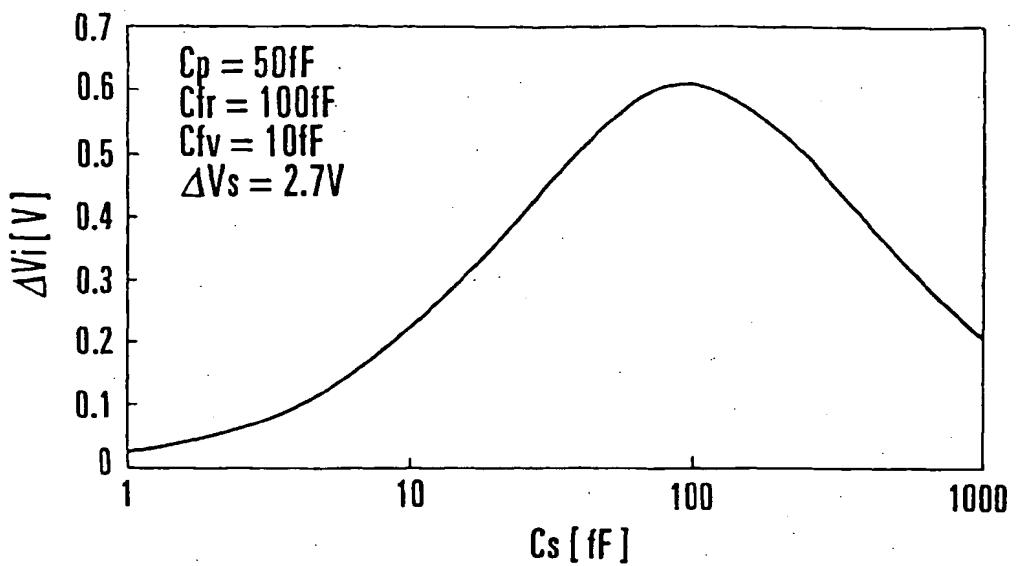


FIG. 24

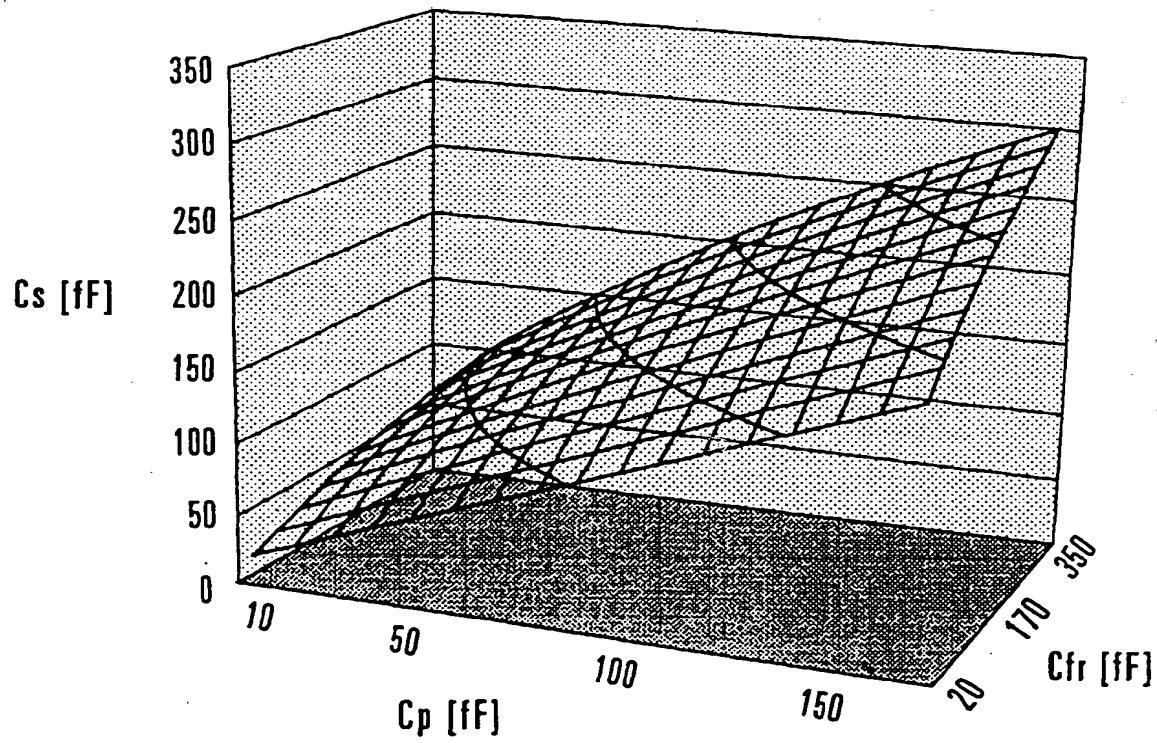


FIG. 25

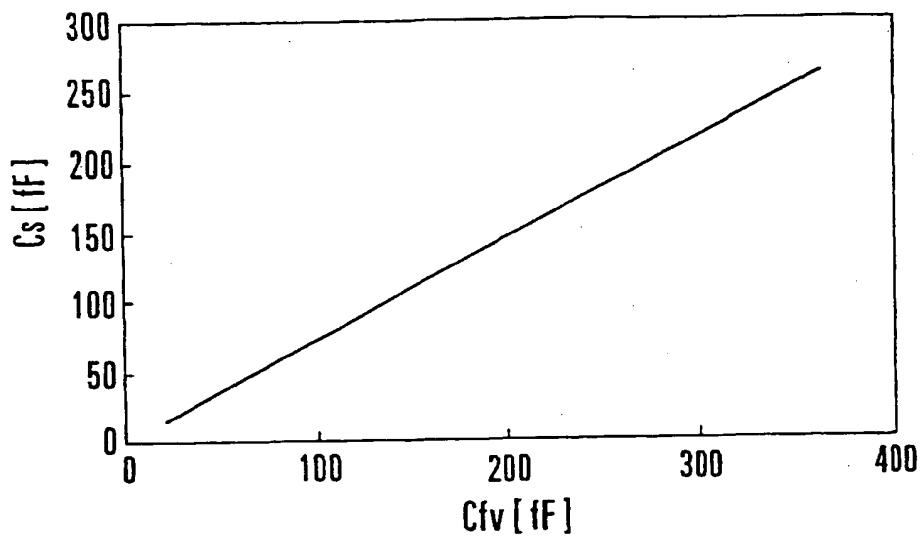


FIG. 26

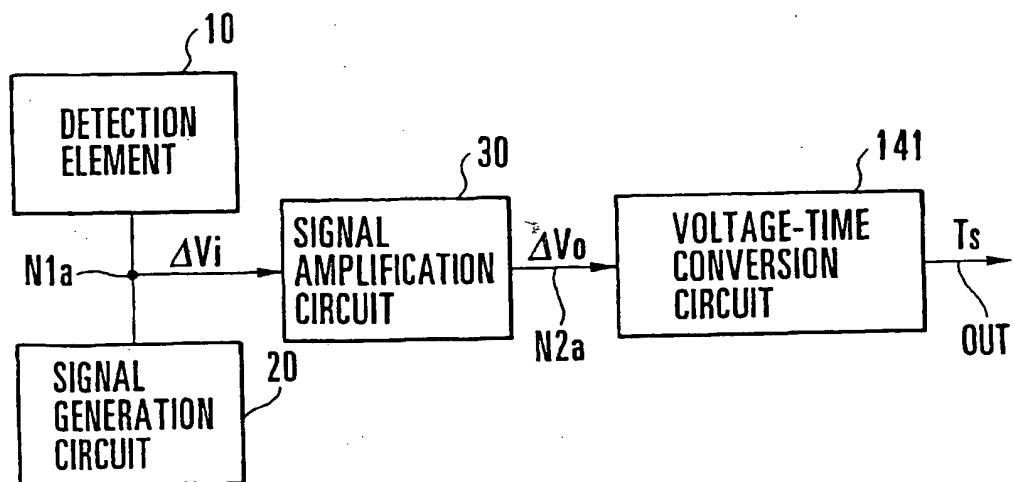
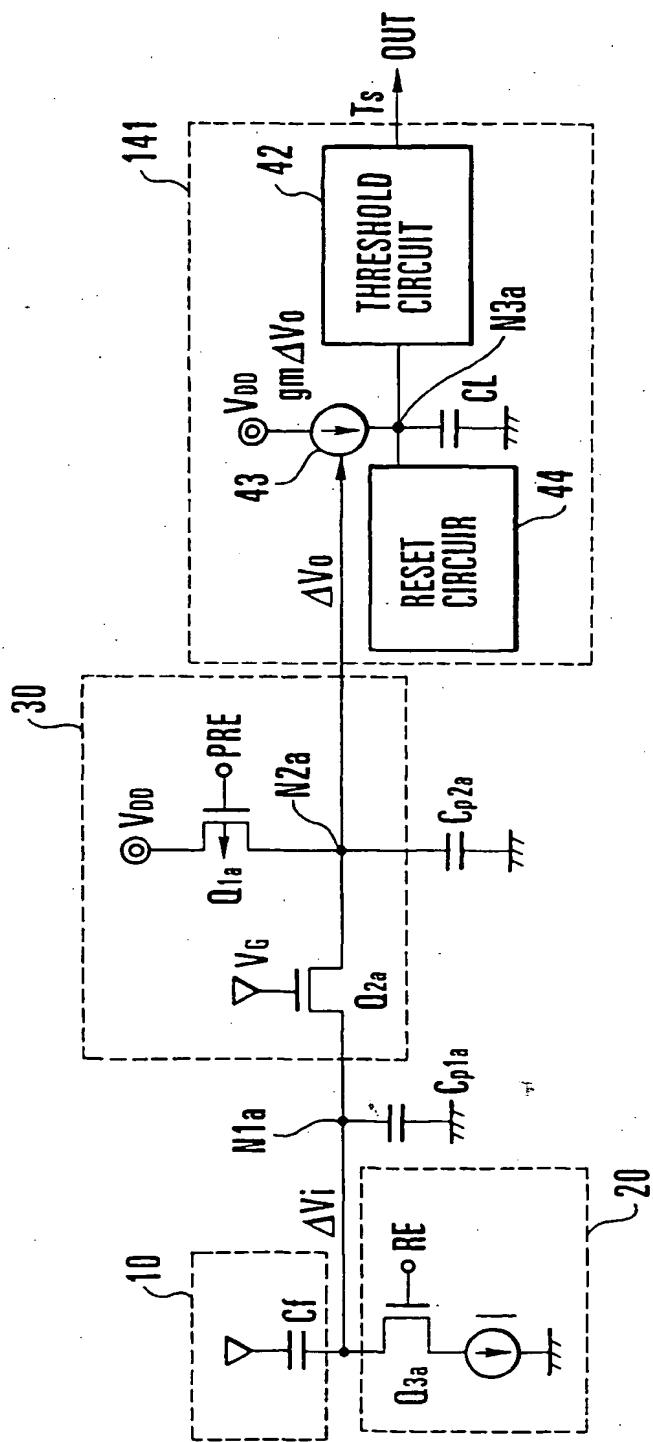


FIG. 27

FIG. 28



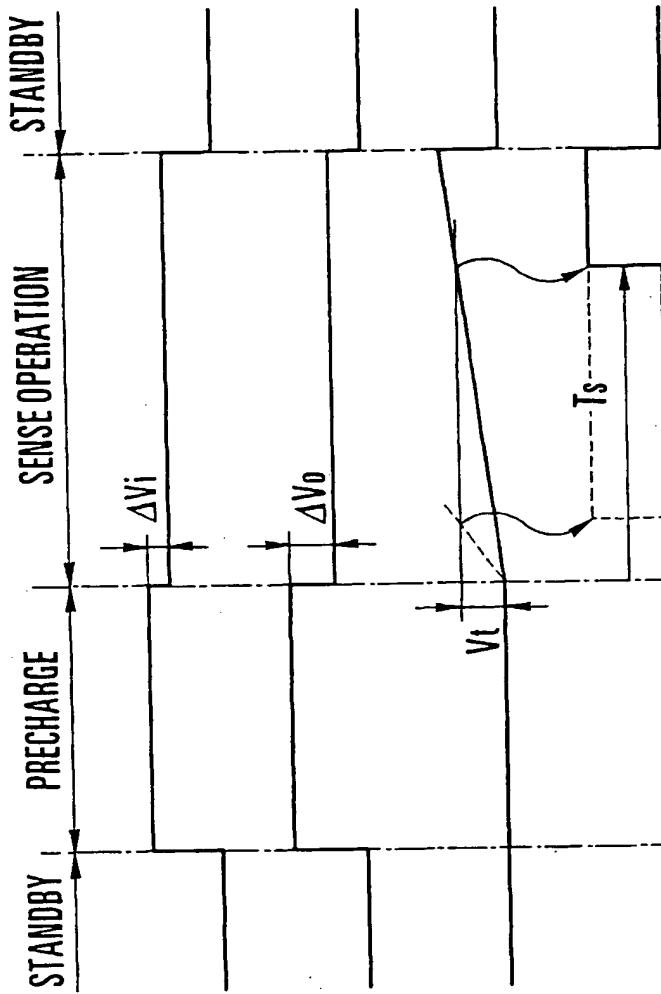


FIG. 29A
POTENTIAL AT N1a

FIG. 29B
POTENTIAL AT N2a

FIG. 29C
POTENTIAL AT N3a

FIG. 29D
POTENTIAL AT OUT

$$T_s = \frac{C_L \cdot V_t}{g_m \Delta V_0} \propto 1/C_L \propto \frac{1}{f}$$

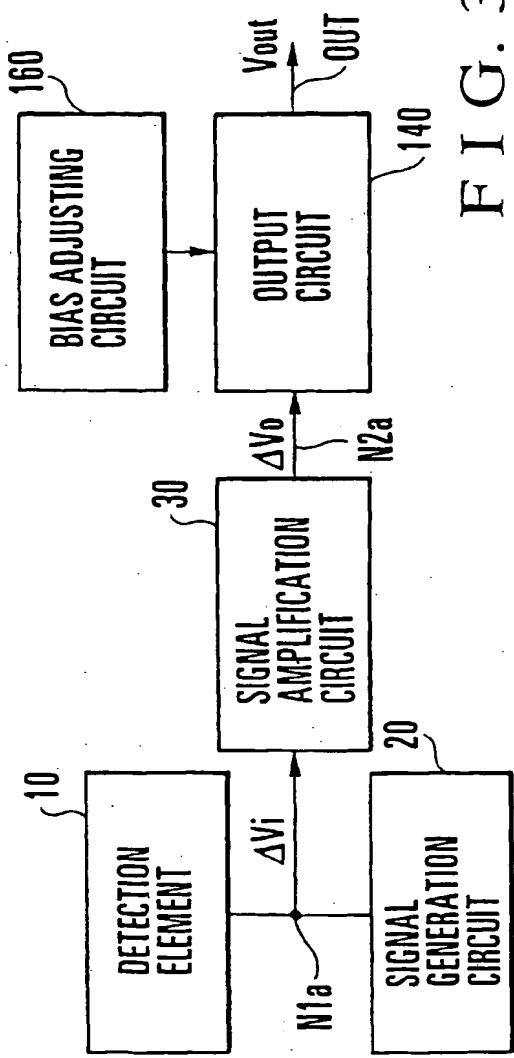


FIG. 30

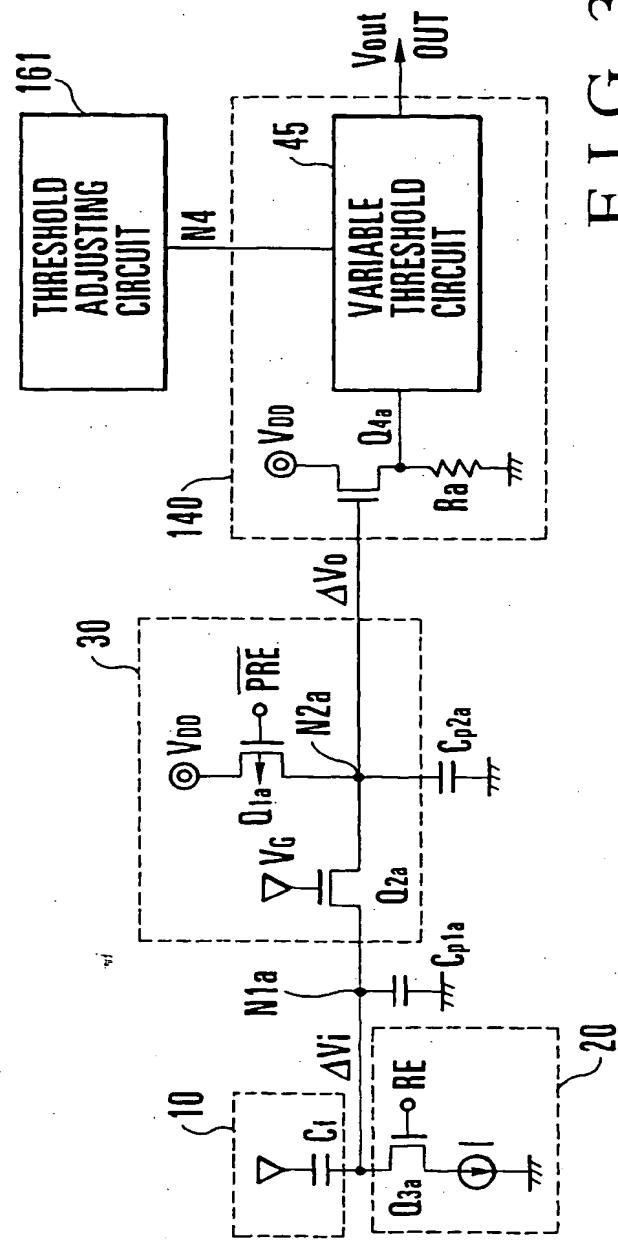


FIG. 31

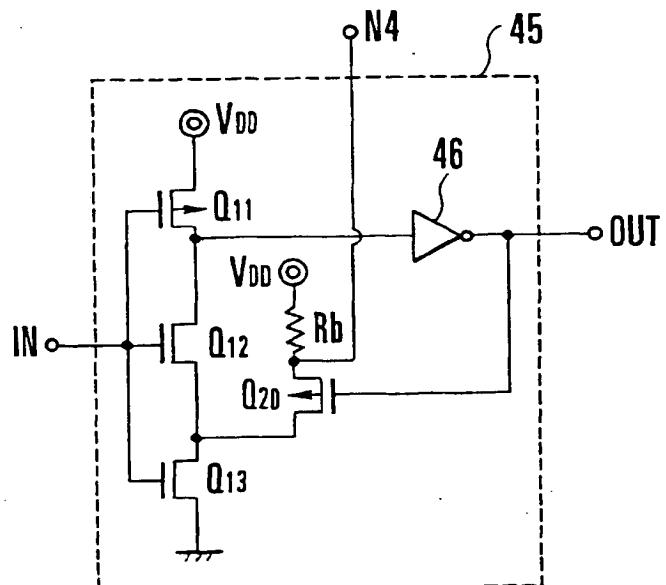


FIG. 32

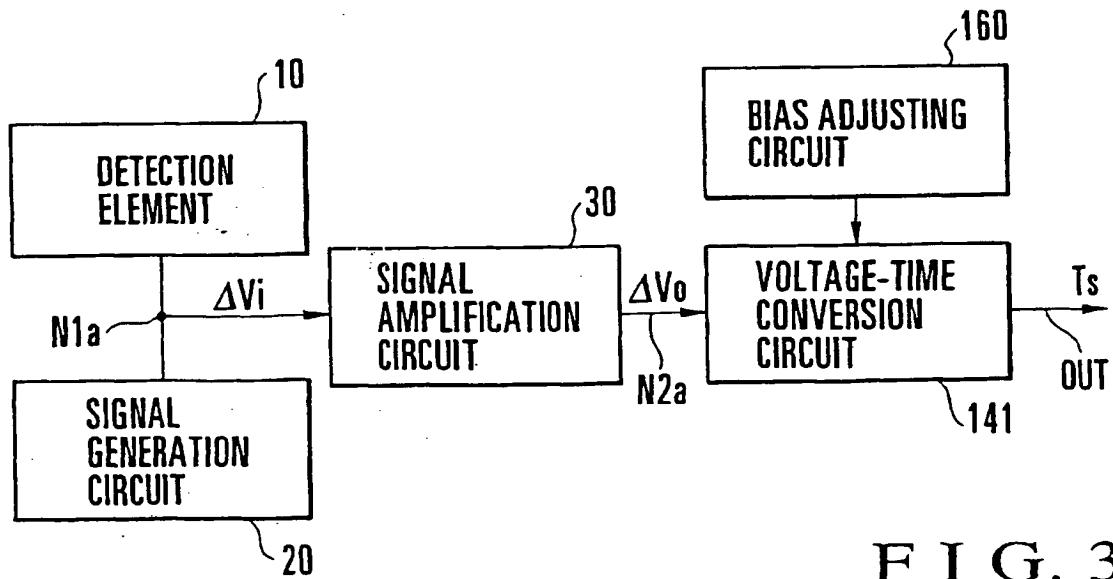


FIG. 33

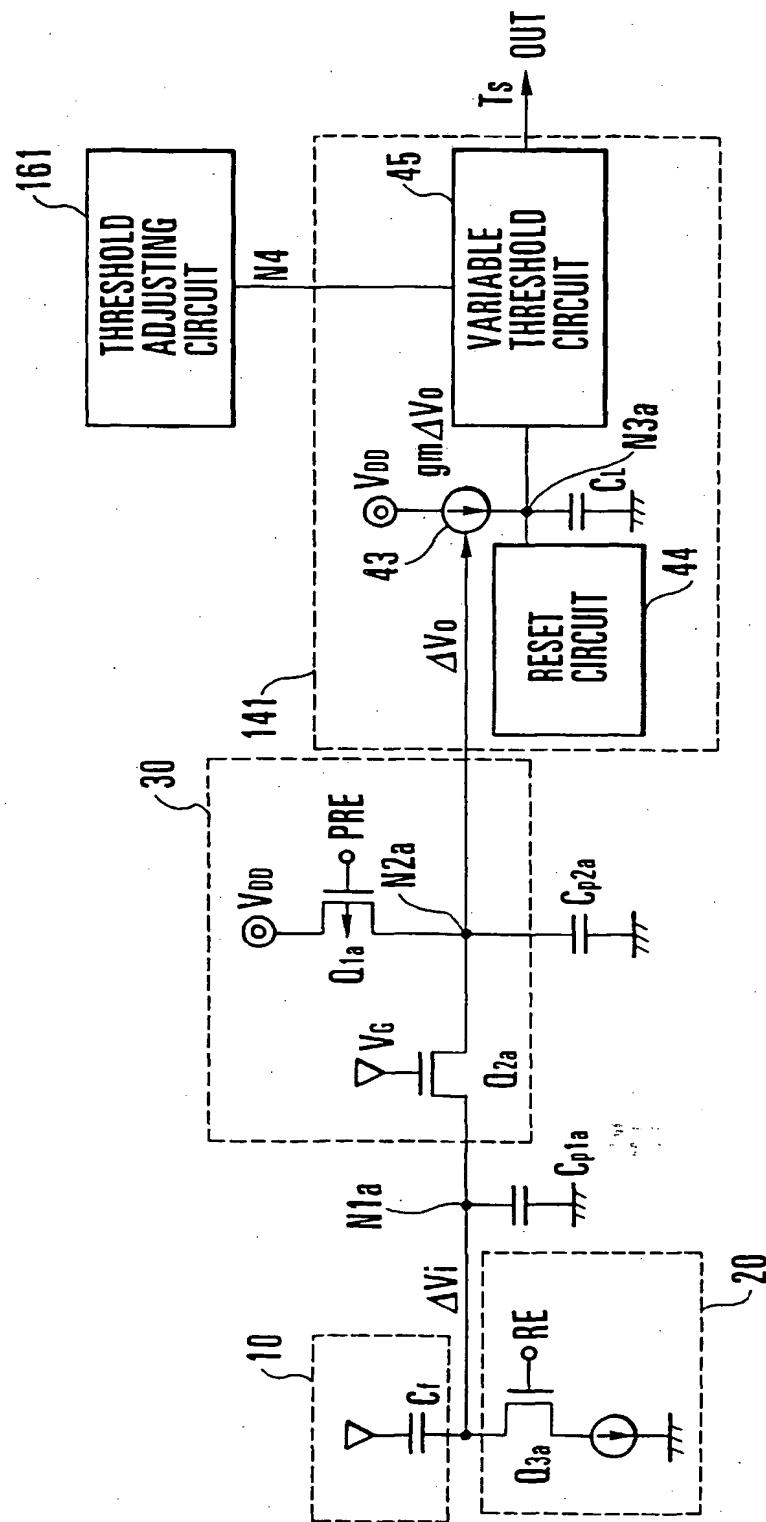


FIG. 34

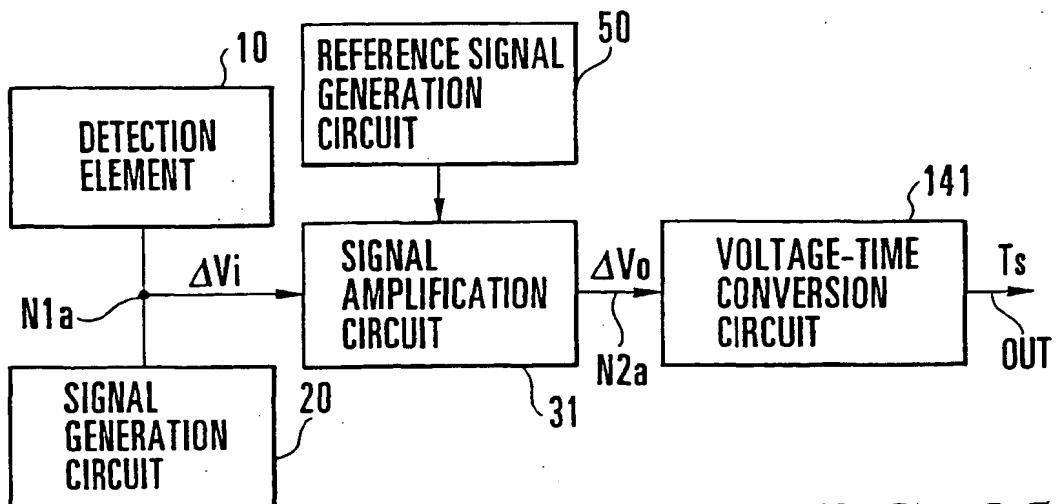


FIG. 35

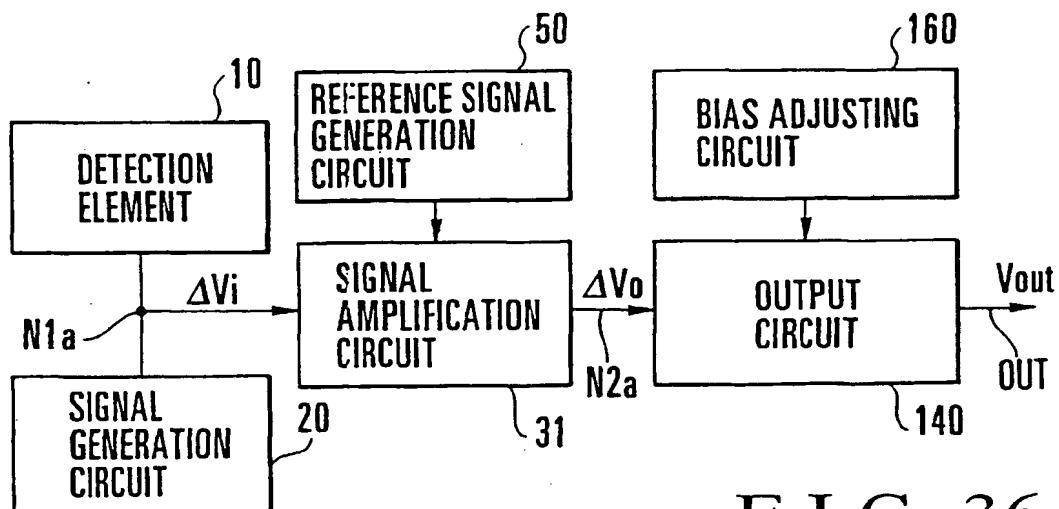


FIG. 36

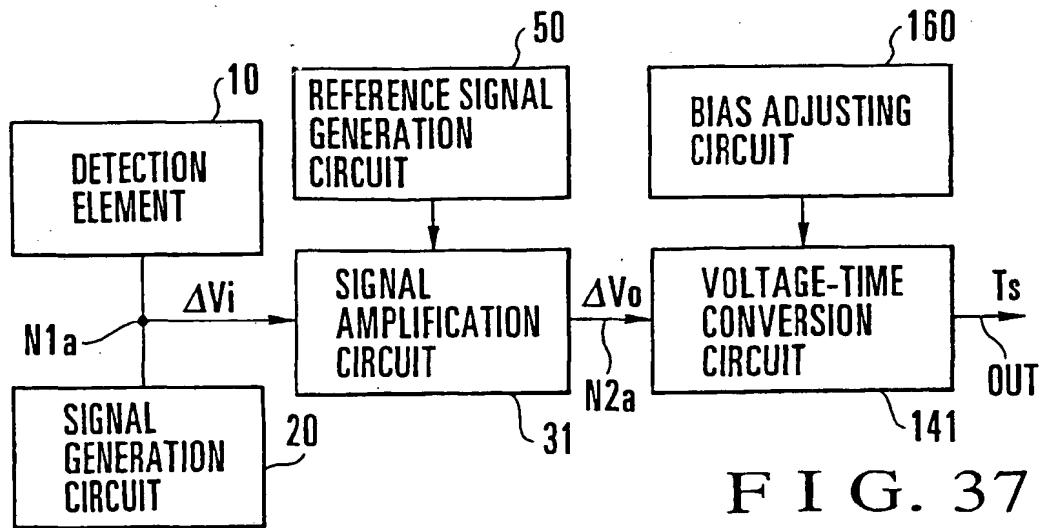


FIG. 37

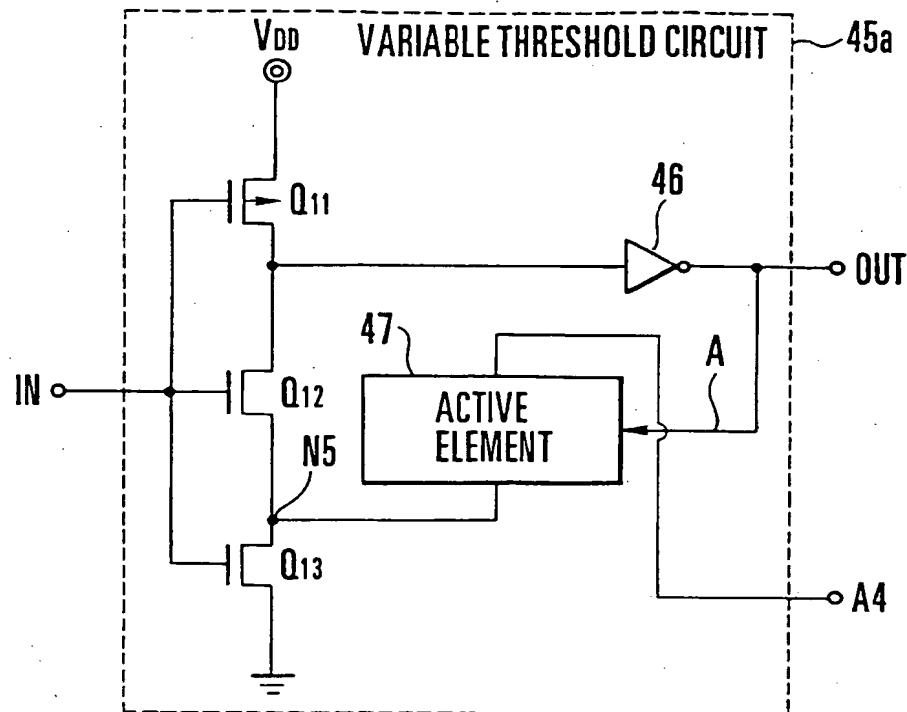


FIG. 38

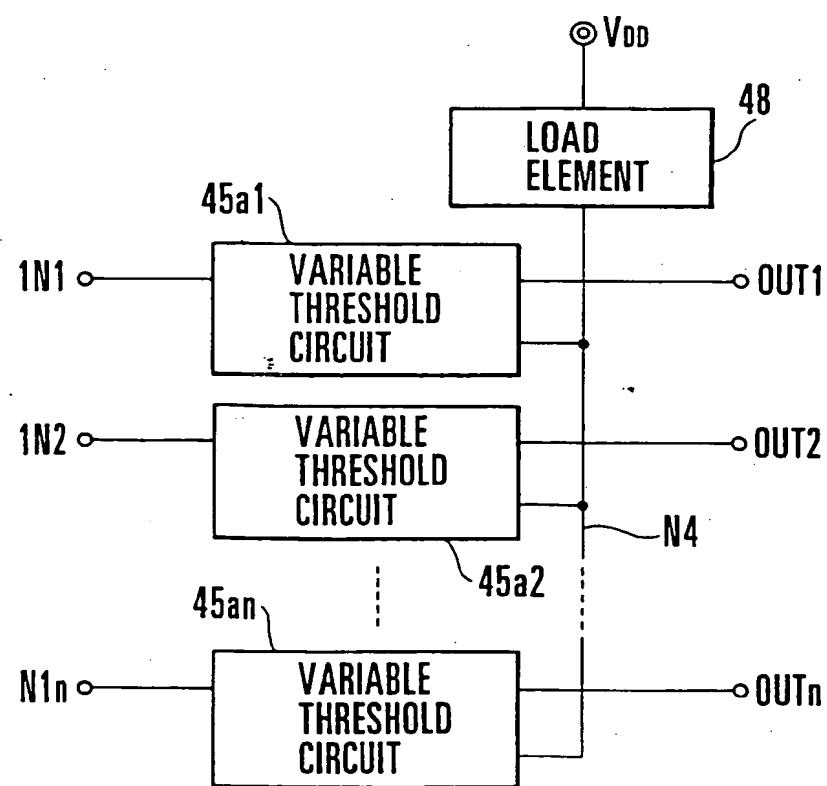


FIG. 39

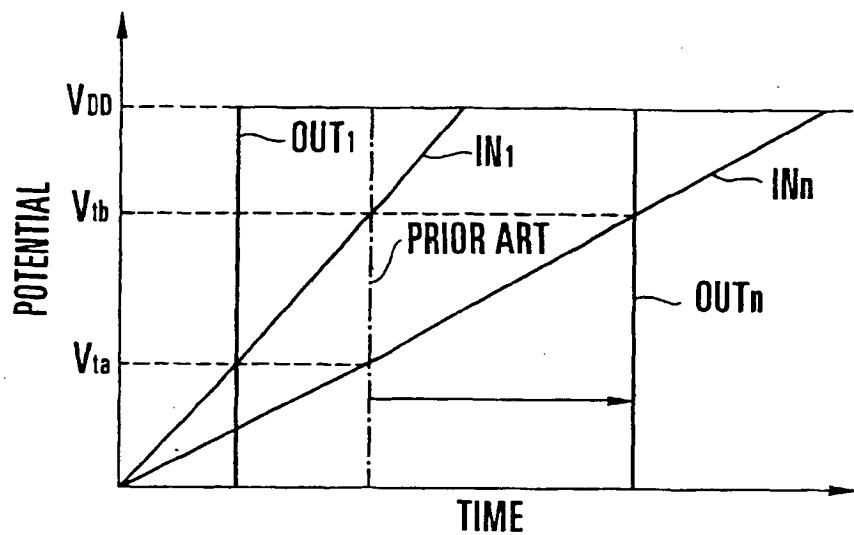


FIG. 40

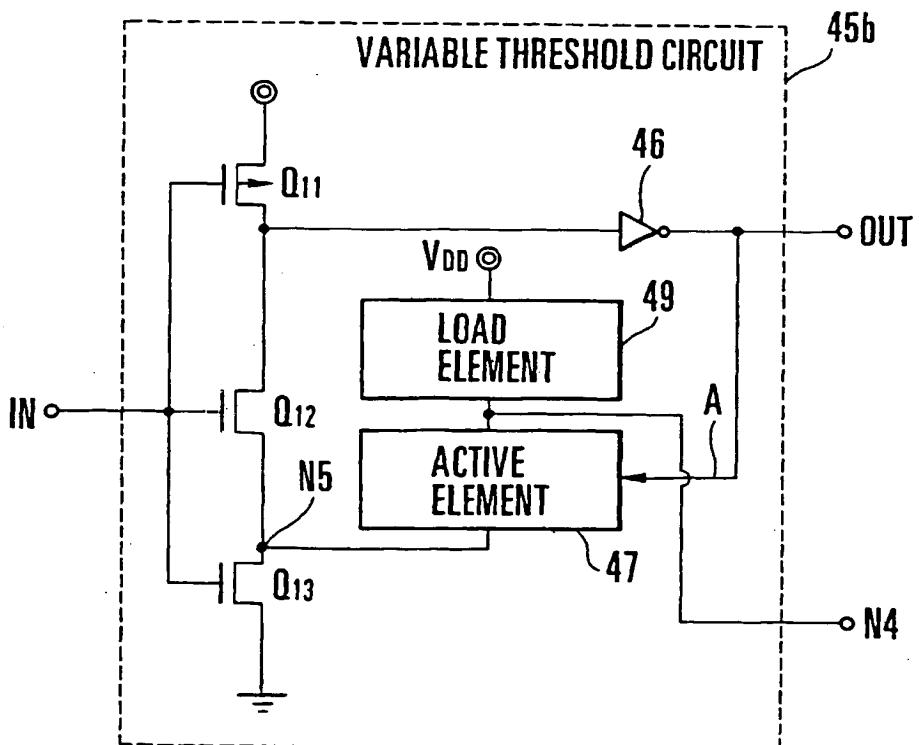
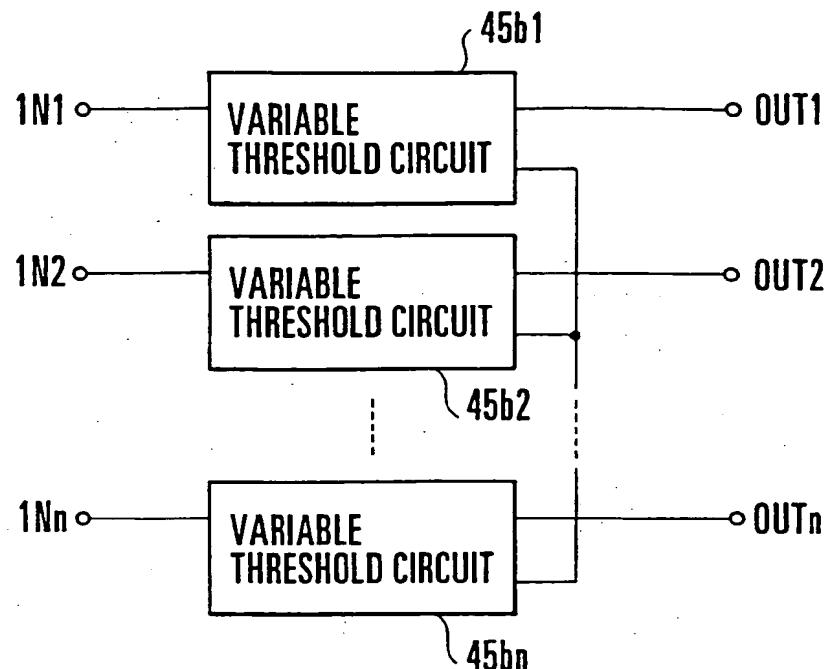
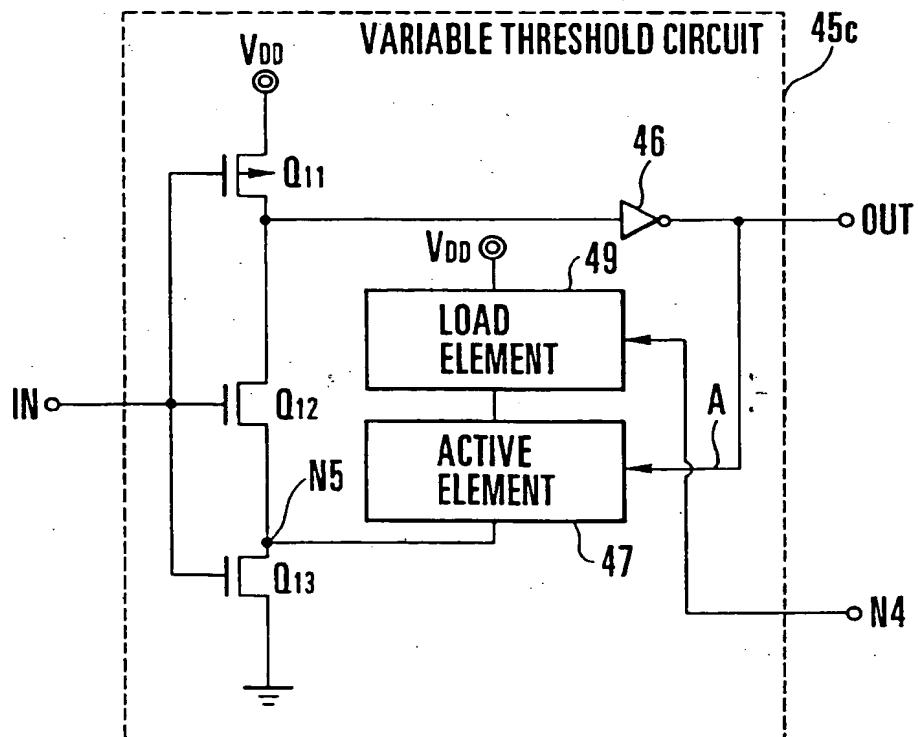


FIG. 41



F I G. 42



F I G. 43

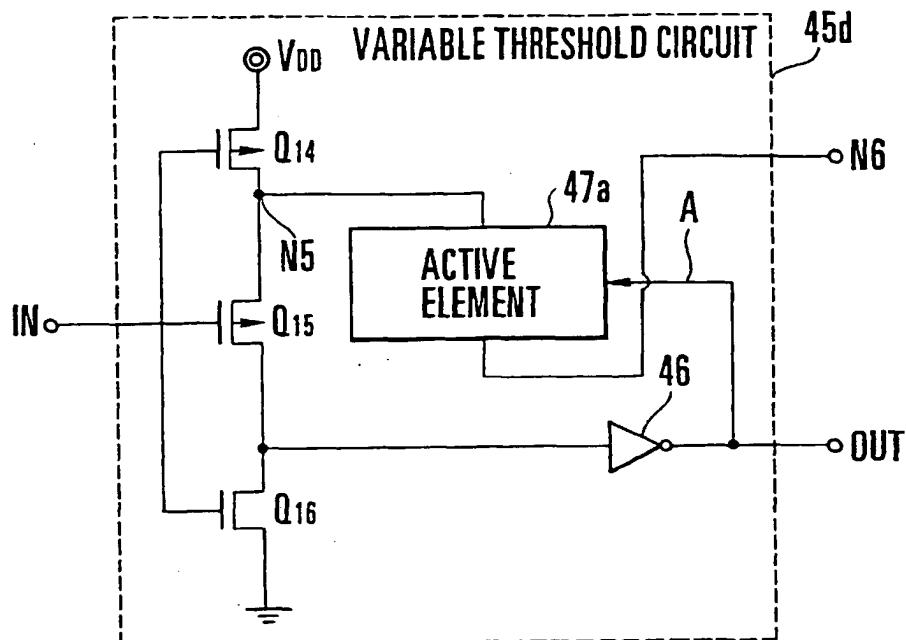


FIG. 44

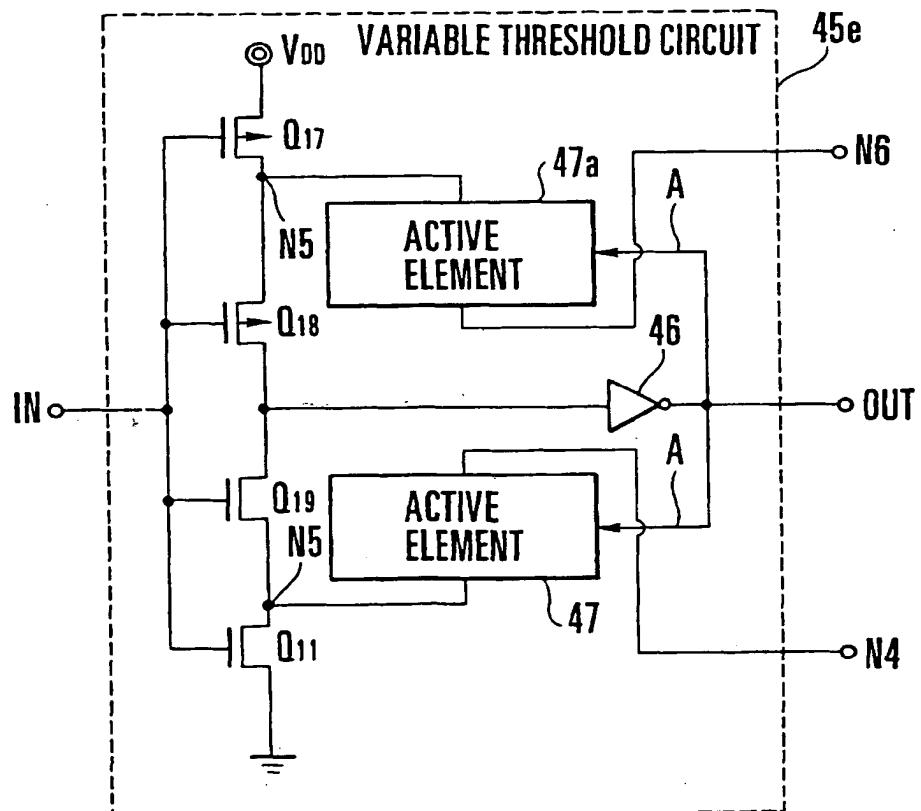


FIG. 45

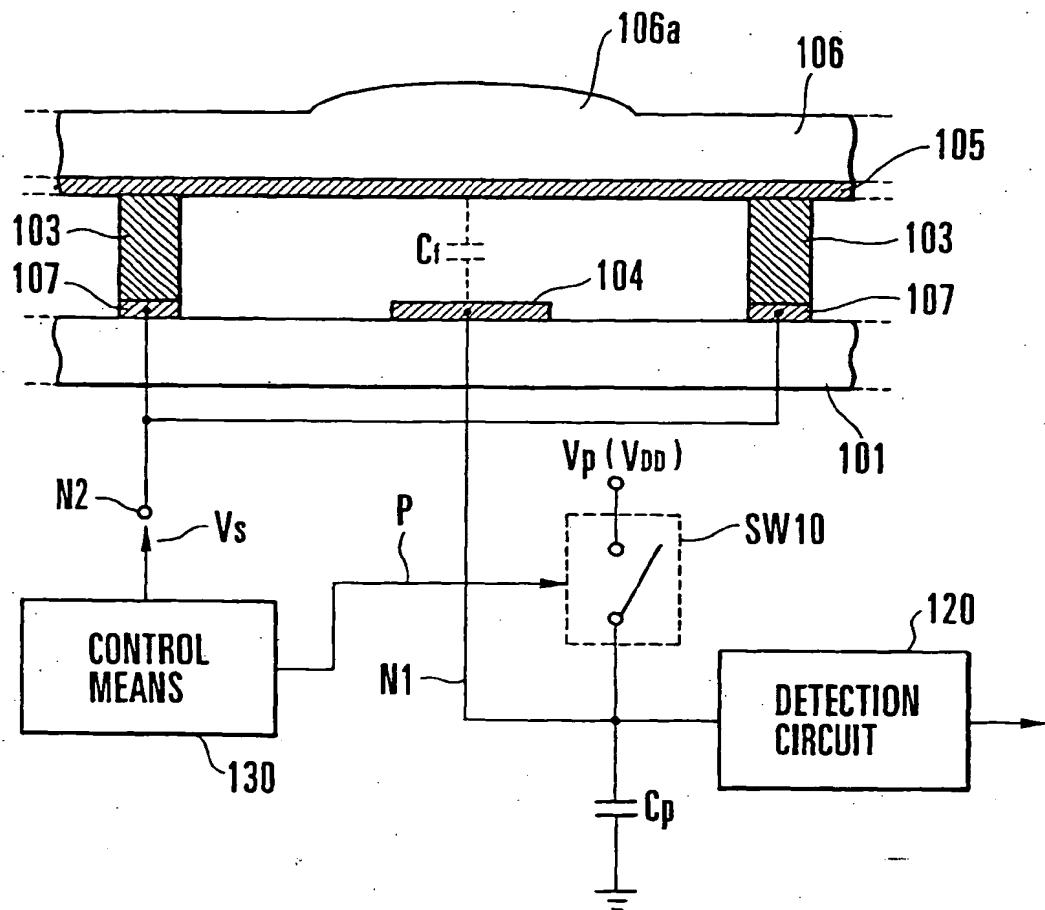


FIG. 46

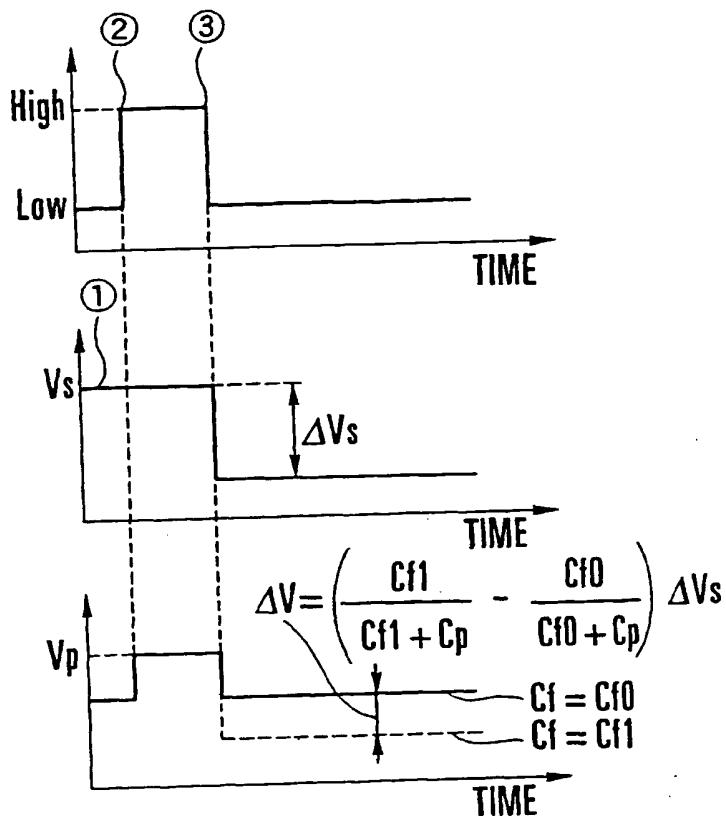
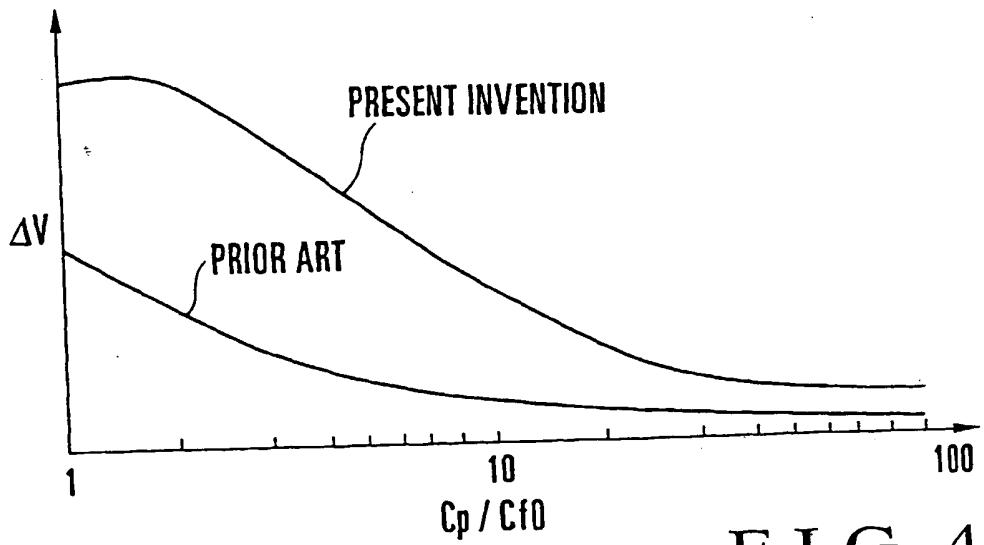
FIG. 47A
POTENTIAL PFIG. 47C
POTENTIAL AT N1

FIG. 48

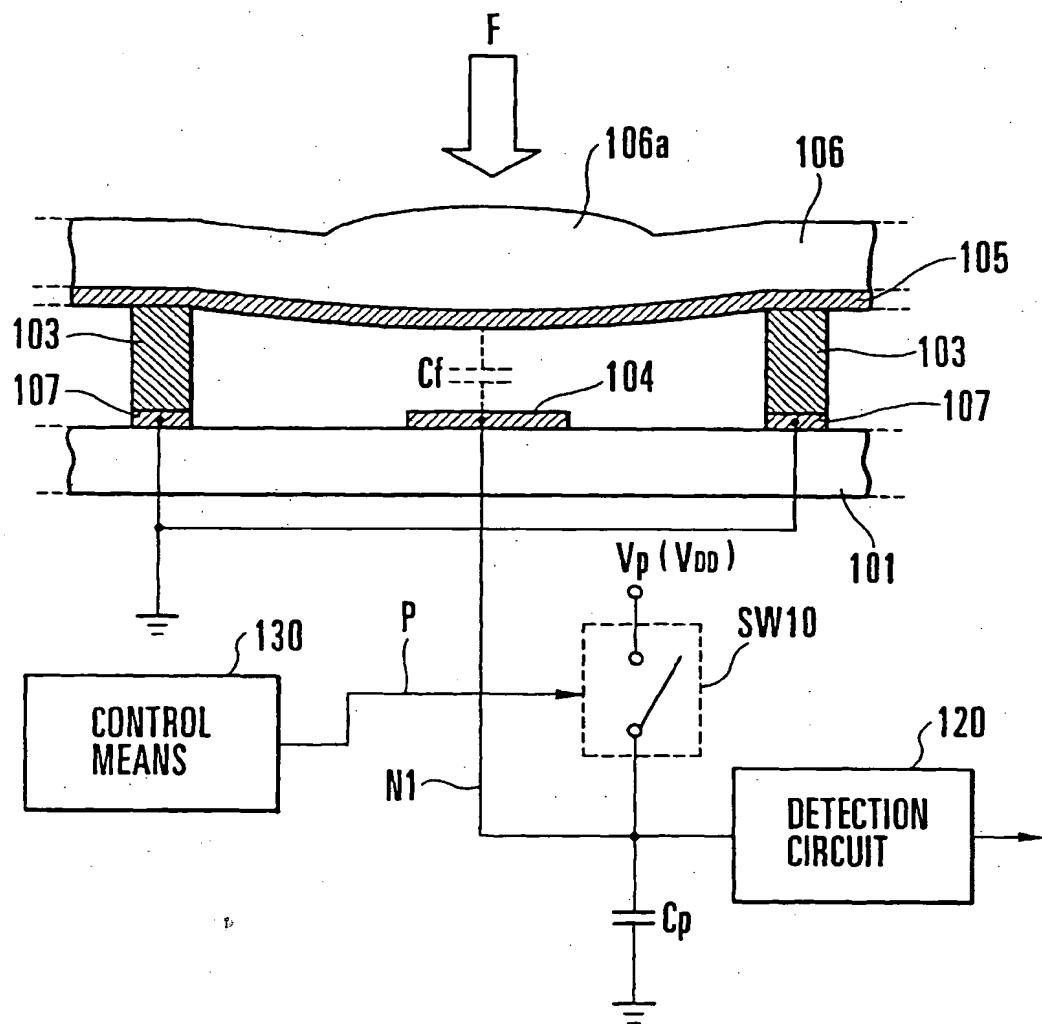


FIG. 49

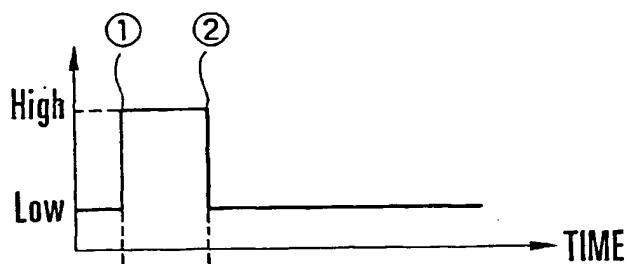
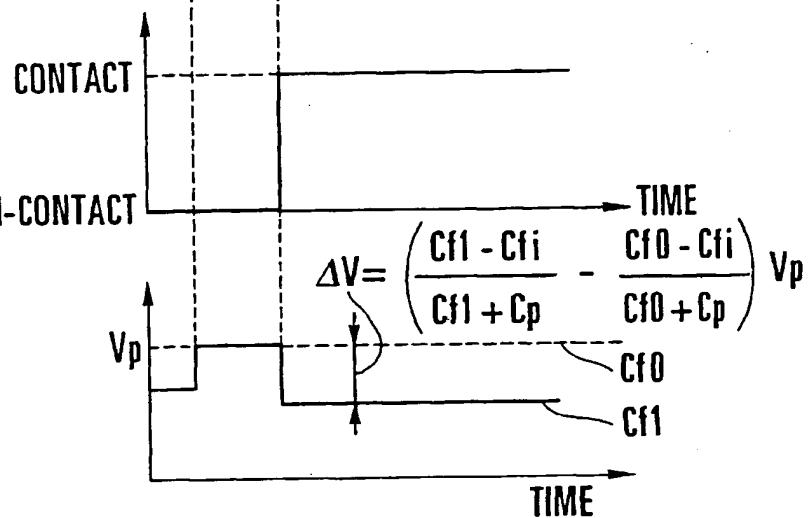
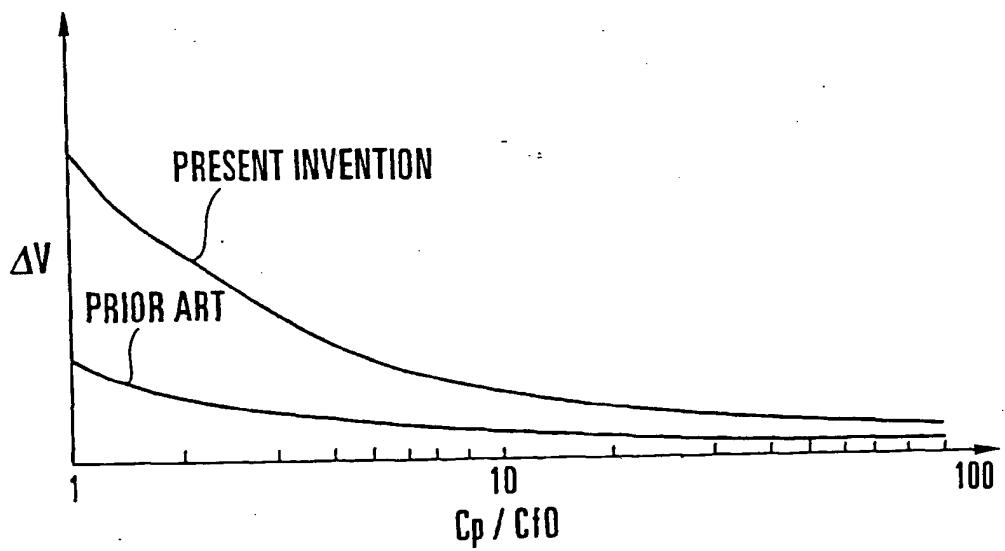
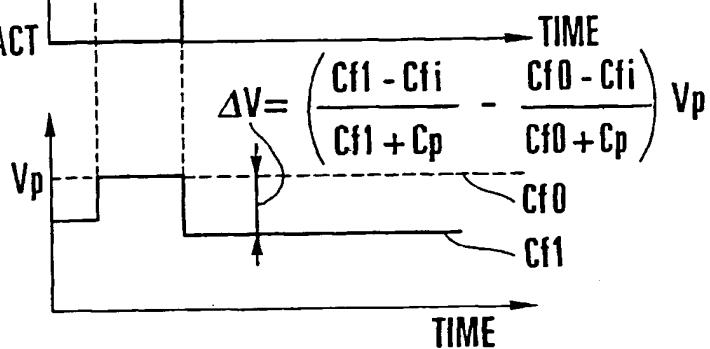
FIG. 50A
POTENTIAL PFIG. 50B
STATE OFFFIG. 50C
POTENTIAL AT N1

FIG. 51

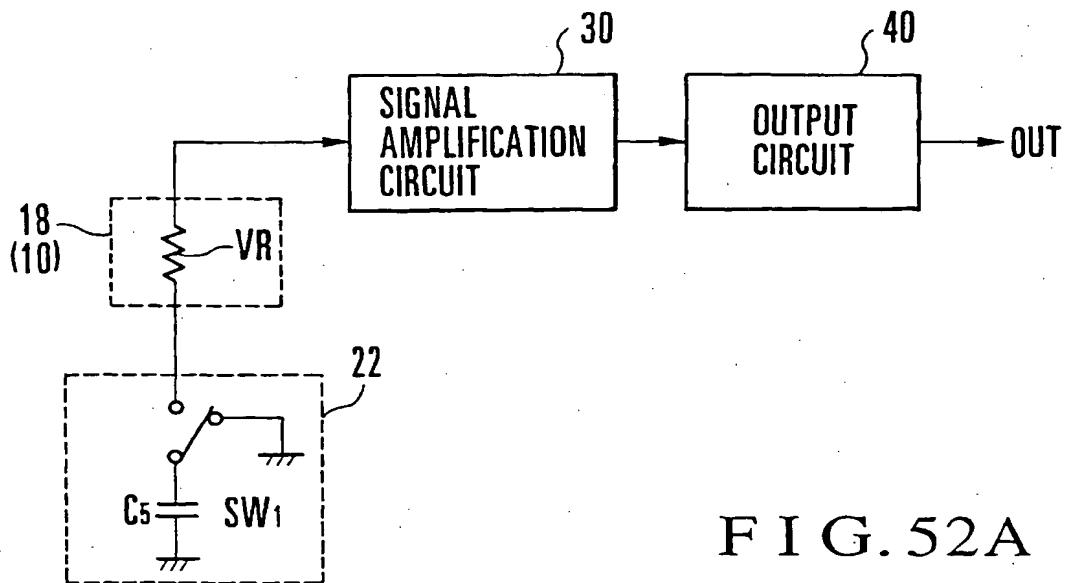


FIG. 52A

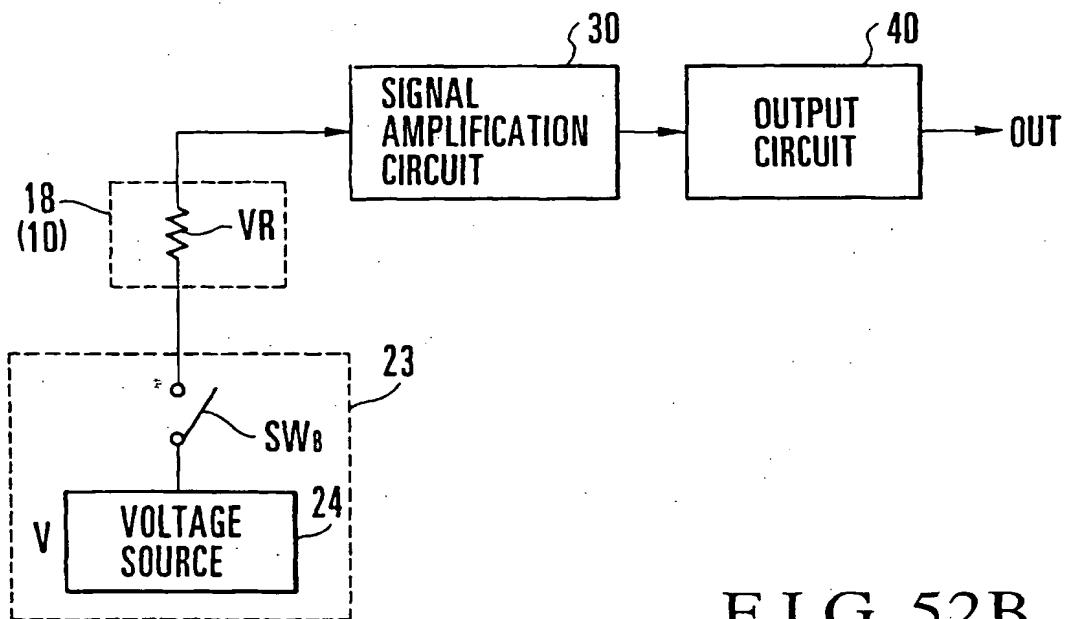


FIG. 52B

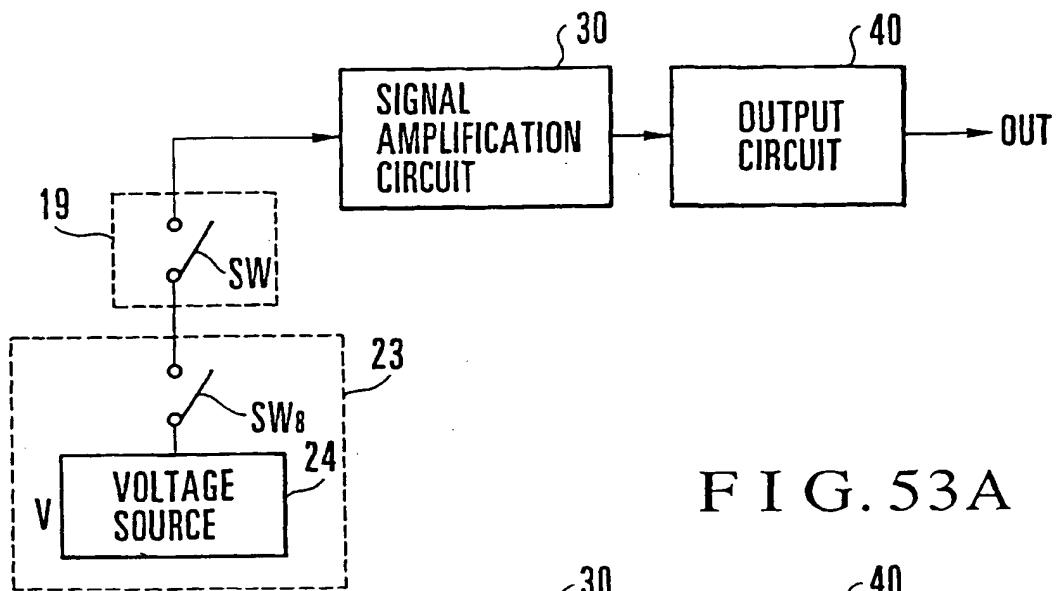


FIG. 53A

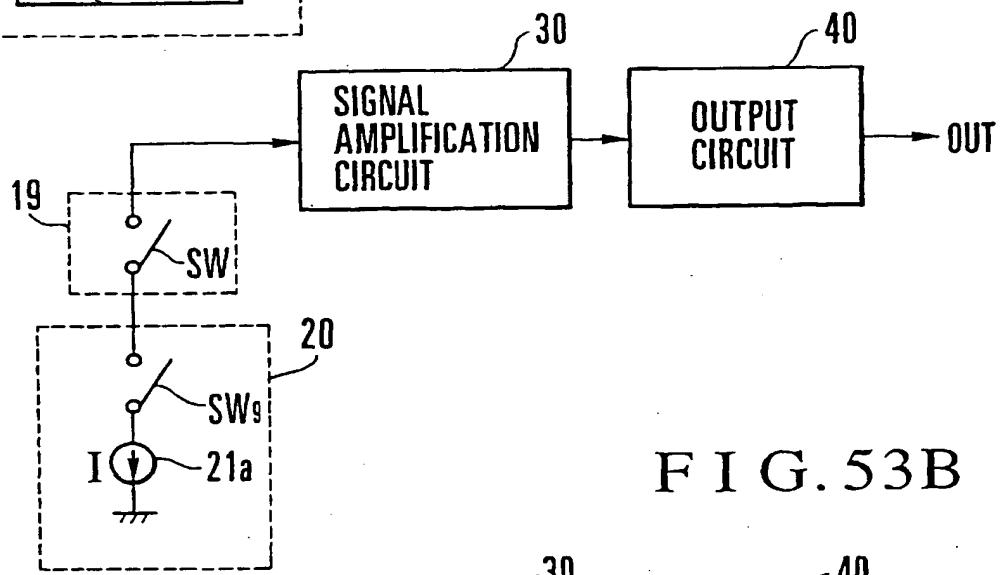


FIG. 53B

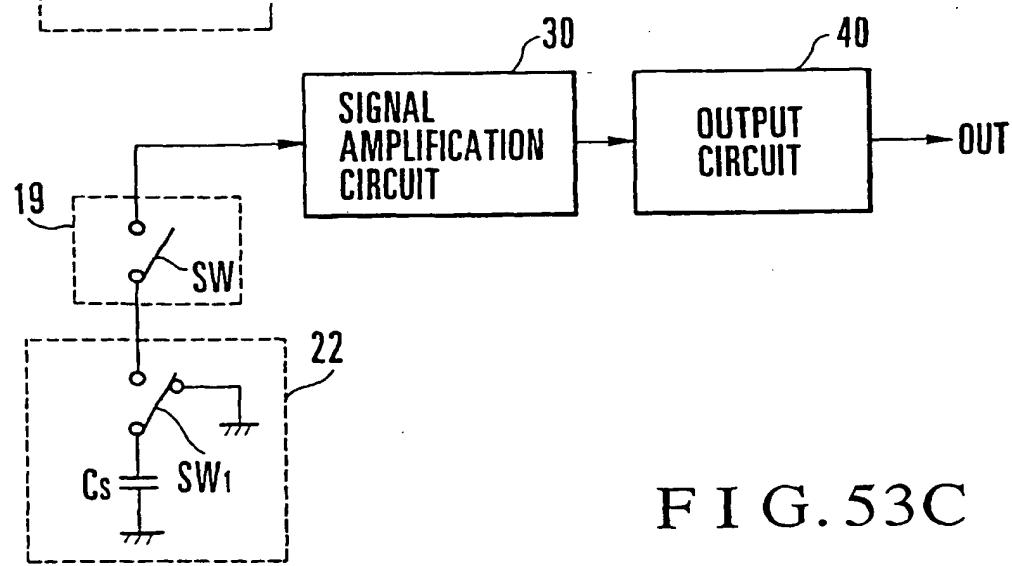
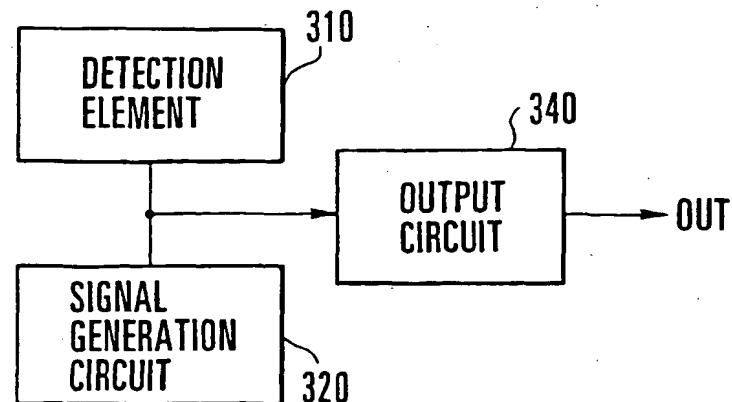
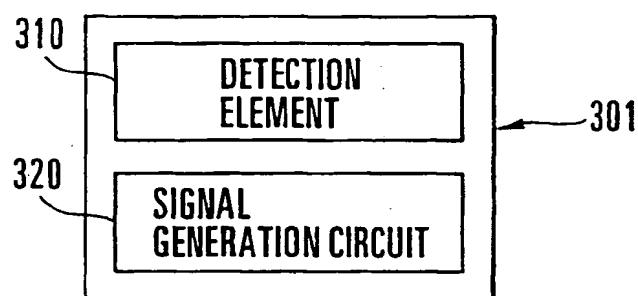


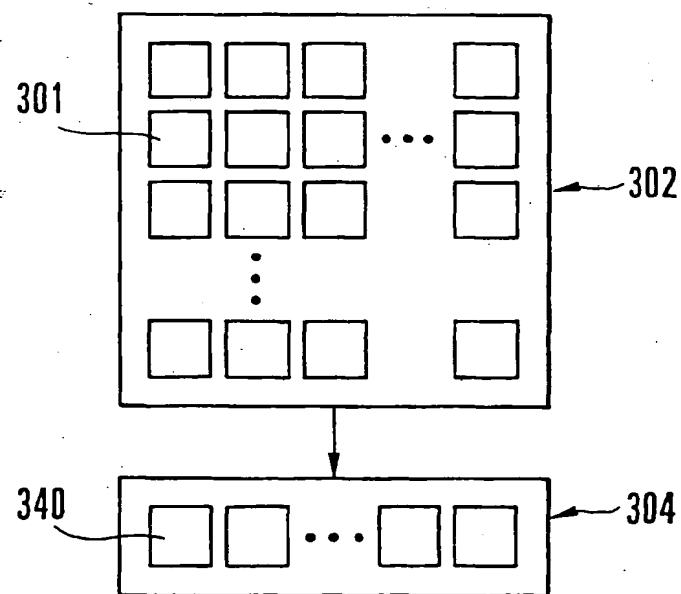
FIG. 53C



F I G. 54



F I G. 55A



F I G. 55B

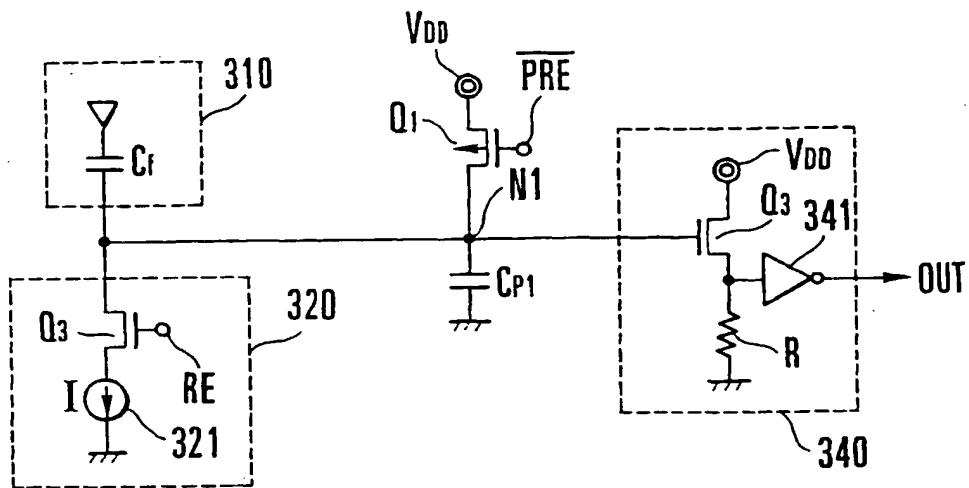


FIG. 56

FIG. 57 A



FIG. 57 B

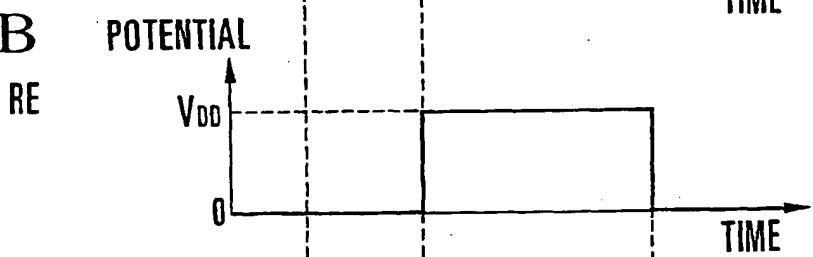
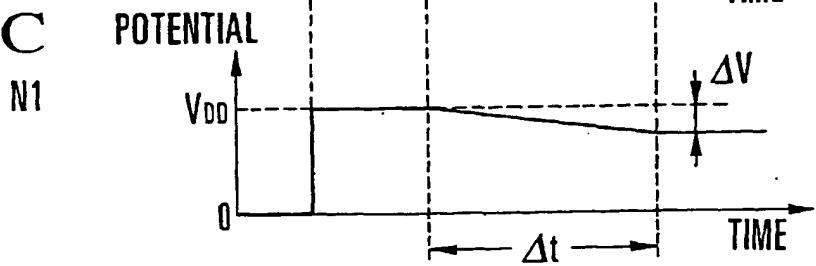


FIG. 57 C





DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (Int.Cl.7)		
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)		
X	EP 0 779 497 A (LUCENT TECHNOLOGIES INC) 18 June 1997 (1997-06-18)	52,55, 56,59 1,60	G11C11/24 G11C27/02 G06K9/00 G01R27/26		
A	* column 3, line 21 - line 56 * * figures 1,2 *				
Y	MARIOLI D ET AL: "MEASUREMENT OF SMALL CAPACITANCE VARIATIONS" IEEE TRANSACTIONS ON INSTRUMENTATION AND MEASUREMENT, vol. 40, no. 2, 1 April 1991 (1991-04-01), pages 426-428, XP000234289 ISSN: 0018-9456	60,61			
A	* page 426, column 1, line 1 - column 2, line 32 * * figure 1 *	1			
Y	US 5 325 442 A (KNAPP ALAN G) 28 June 1994 (1994-06-28)	60,61			
A	* abstract * * column 7, line 21 - column 8, line 57 * * figure 5 *	1,52,56	TECHNICAL FIELDS SEARCHED (Int.Cl.7)		
		-/-	G11C G06K G01R		
The present search report has been drawn up for all claims					
Place of search	Date of completion of the search	Examiner			
THE HAGUE	25 October 1999	Colling, P			
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Application Number
EP 99 25 0215

DOCUMENTS CONSIDERED TO BE RELEVANT									
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)						
A	<p>DATABASE INSPEC [Online] INSTITUTE OF ELECTRICAL ENGINEERS, STEVENAGE, GB REY P ET AL: "A high density capacitive pressure sensor array for fingerprint sensor application" Database accession no. 5773806 XP002119967 * abstract * & TRANSDUCERS 97. 1997 INTERNATIONAL CONFERENCE ON SOLID-STATE SENSORS AND ACTUATORS. DIGEST OF TECHNICAL PAPERS (CAT. NO.97TH8267), PROCEEDINGS OF INTERNATIONAL SOLID STATE SENSORS AND ACTUATORS CONFERENCE (TRANSDUCERS '97), CHICAGO, IL, USA, 16-19 JUN, pages 1453-1456 vol.2, 1997, New York, NY, USA, IEEE, USA ISBN: 0-7803-3829-4 * page 1453, column 1, line 1 - column 2, line 10 * * figure 1 *</p> <p>---</p> <p>-/-</p>	56,59							
				TECHNICAL FIELDS SEARCHED (Int.Cl.7)					
<p>The present search report has been drawn up for all claims</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 33%;">Place of search</td> <td style="width: 33%;">Date of completion of the search</td> <td style="width: 34%;">Examiner</td> </tr> <tr> <td>THE HAGUE</td> <td>25 October 1999</td> <td>Colling, P</td> </tr> </table> <p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document</p>				Place of search	Date of completion of the search	Examiner	THE HAGUE	25 October 1999	Colling, P
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D,A	<p>DATABASE INSPEC [Online] INSTITUTE OF ELECTRICAL ENGINEERS, STEVENAGE, GB INGLIS C ET AL: "A robust, 1.8 V 250 μW direct-contact 500 dpi fingerprint sensor" Database accession no. 5999084 XP002119968 * abstract * & 1998 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE. DIGEST OF TECHNICAL PAPERS, ISSCC. FIRST EDITION (CAT. NO. 98CH36156), 1998 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE. DIGEST OF TECHNICAL PAPERS. ISSCC, SAN FRANCISCO, CA, USA, 5-7 FEB, pages 284-285, 1998, New York, NY, USA, IEEE, USA ISBN: 0-7803-4344-1 * the whole document *</p> <p>---</p> <p>WO 98 52135 A (VERIDICOM INC) 19 November 1998 (1998-11-19)</p> <p>* page 1, line 1 - page 8, line 8 * * page 14, line 6 - page 19, line 13 * * figures 6,7 *</p> <p>---</p> <p>-/-</p>	1,52,56, 60							
P,X		52,55,	TECHNICAL FIELDS SEARCHED (Int.Cl.7)						
P,A		56,59-61 1							
<p>The present search report has been drawn up for all claims</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 33%;">Place of search</td> <td style="width: 33%;">Date of completion of the search</td> <td style="width: 34%;">Examiner</td> </tr> <tr> <td>THE HAGUE</td> <td>25 October 1999</td> <td>Colling, P</td> </tr> </table>				Place of search	Date of completion of the search	Examiner	THE HAGUE	25 October 1999	Colling, P
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P,A	<p>DATABASE INSPEC [Online] INSTITUTE OF ELECTRICAL ENGINEERS, STEVENAGE, GB JEONG-WOO LEE ET AL: "A 600-dpi capacitive fingerprint sensor chip and image-synthesis technique" Database accession no. 6222869 XP002119969 * abstract * & IEEE JOURNAL OF SOLID-STATE CIRCUITS, APRIL 1999, IEEE, USA, vol. 34, no. 4, pages 469-475, ISSN: 0018-9200 * page 470, column 2, paragraph 2 - page 471, column 2, paragraph 6 * * figures 4-6 *</p> <p>-----</p>	1,52,56, 60	
			TECHNICAL FIELDS SEARCHED (Int.Cl.7)
<p>The present search report has been drawn up for all claims</p>			
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